

COMPAL CONFIDENTIAL

MODEL NAME : QXW00
PCB NO : LA-7901P (DA60000PM00)
BOM P/N : 4619F631L01 / L02
GPIO MAP: E4_VC_GPIO_map_rev_1.1

Korbel 14 UMA--Non vPRO
Ivy/Sandy Bridge + Panther POINT(HM77w/DASH)

2012-03-03


REV : 1.0 (A00)

@ : Nopop Component
CONN@ : Connector Component

MB Type	BOM P/N	
TPM	43*	1@ 3@ 5@
TCM		2@ 4@ 5@
TPM DIS		2@ 3@
HM77 w/o Vpro		
QM77 w/ Vpro		
PCH XDP		PXDP@
HDMI LOGO		46@

MB PCB	
Part Number	Description
DA60000PM00	PCB OLH LA-7901P REV0 M/S UMA

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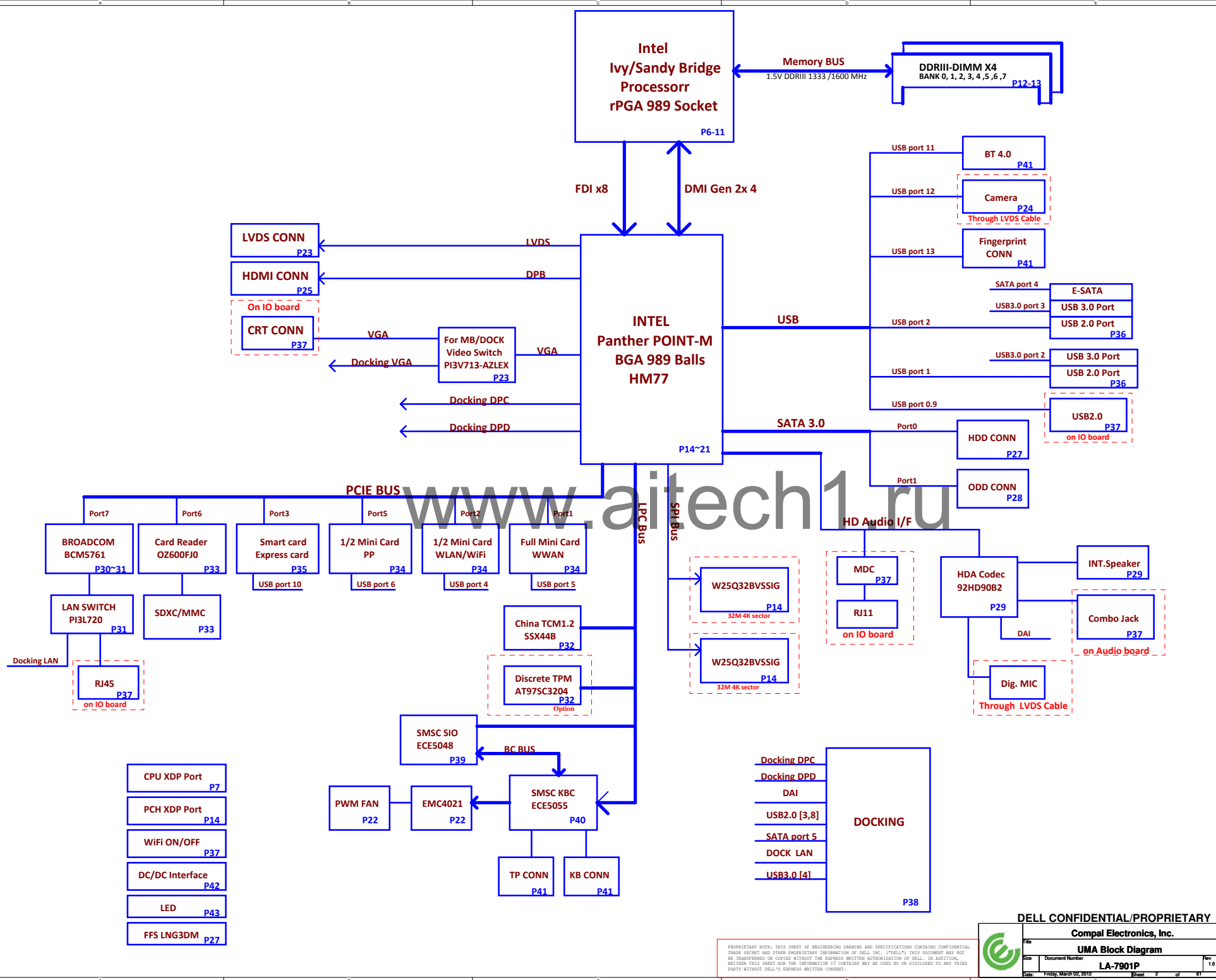


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Cover Sheet

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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

need to update Power Status and
PM Table

USB 3.0 PORT#	Connetion
1	NA
2	JUSB1 (Left side)
3	JUSB2 (Left side)
4	DOCKING

USB PORT#	DESTINATION
0	JUSB (Right side-IO/B)
1	JUSB (Left side)
2	JESA1 (Leftt side ESATA)
3	MLK DOCK
4	WLAN
5	WWAN
*1 6	JMINI3(Flash)-for w/ Vpro
*1 7	DOCKING
8	NA
9	JUSB (Right side-Audio/B)
10	Express card/Smart Card
11	Bluetooth
12	Camera
13	BIO

*1: HM76 don't support port 6,7

SATA	DESTINATION
SATA 0	HDD
SATA 1	ODD/ E3 Module Bay
SATA 2	NA
SATA 3	NA
SATA 4	ESATA
SATA 5	Dock

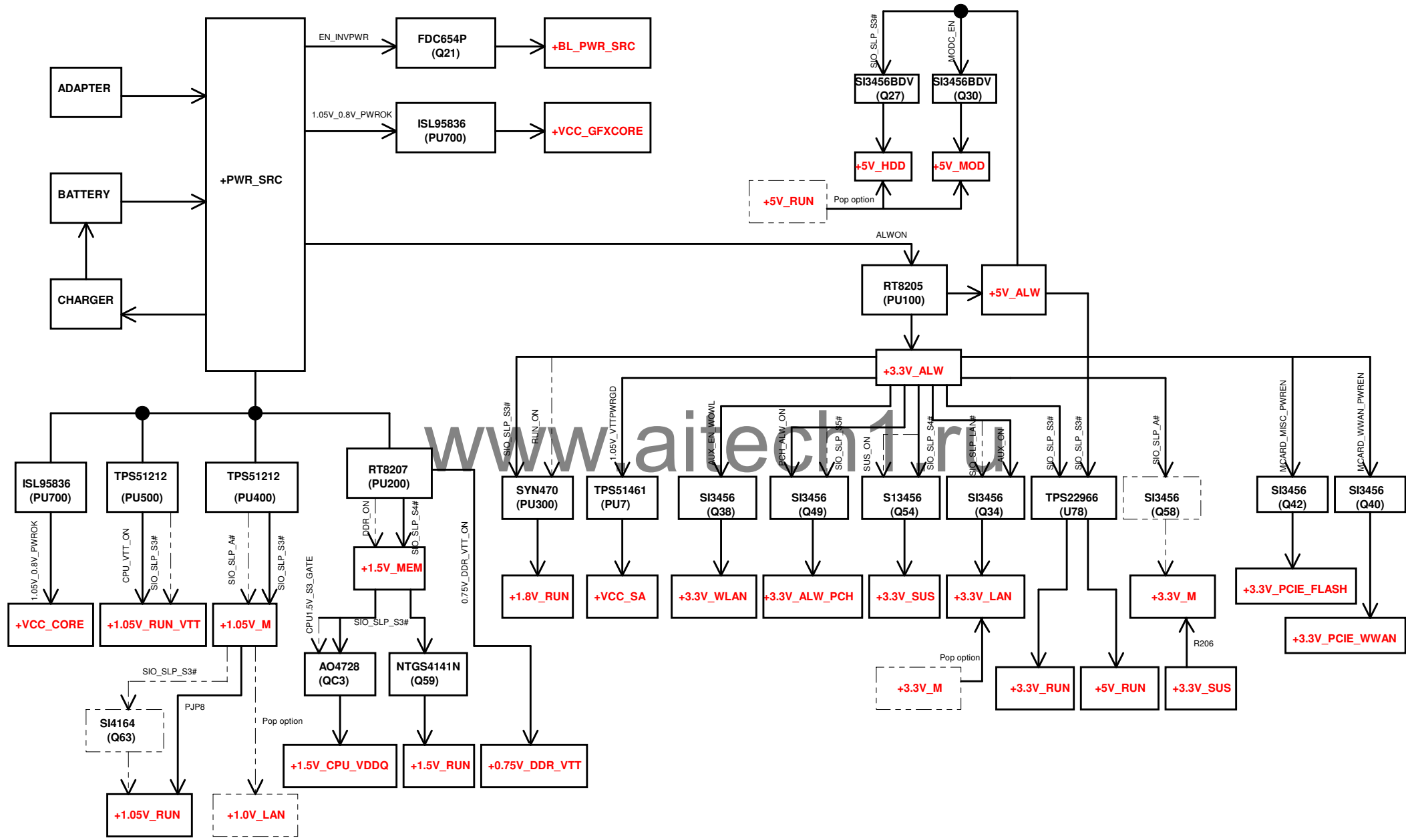
UMA DP/HDMI Port	Connetion
Port B	MB HDMI Conn
Port C	Dock DP port 2
Port D	Dock DP port 1

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	Express card
Lane 4	None
Lane 5	1/2vMINI CARD-3 PCIE
Lane 6	MMI
Lane 7	10/100/1G LOM
Lane 8	None

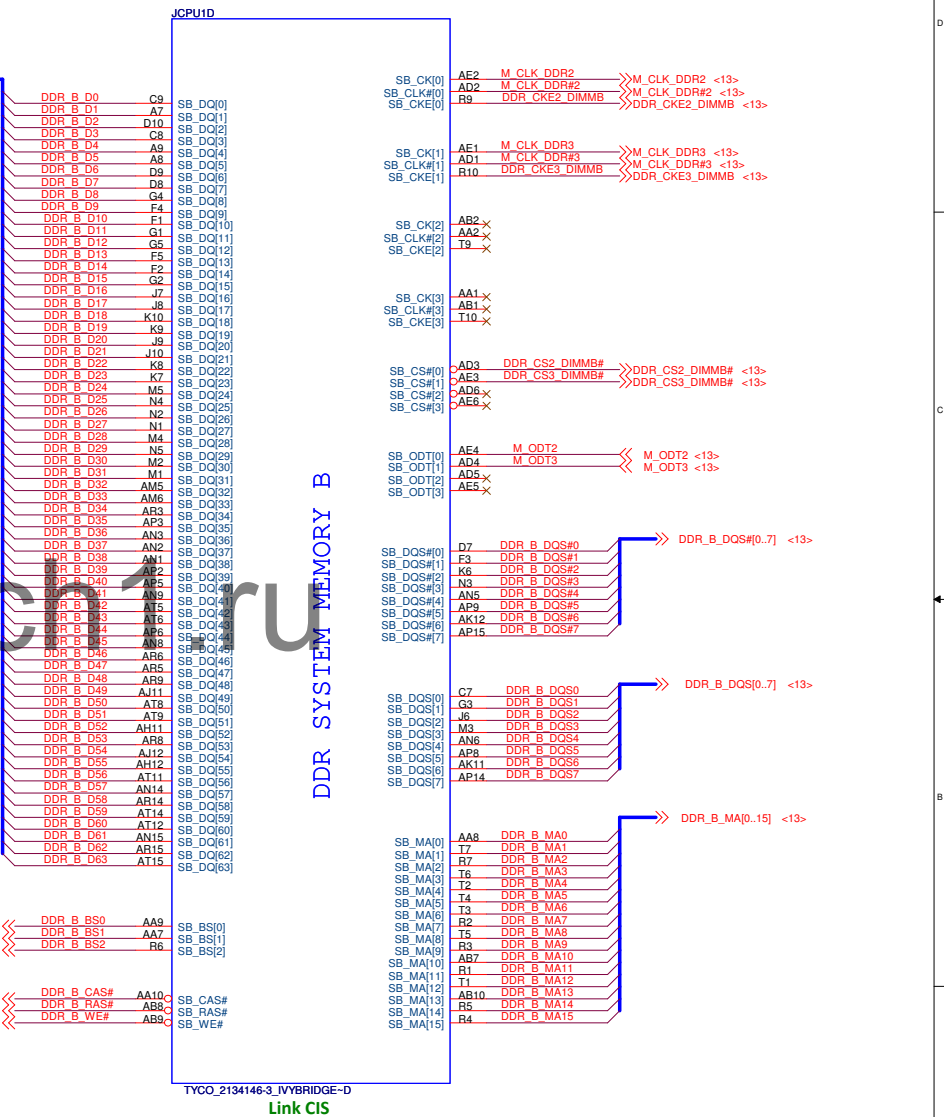
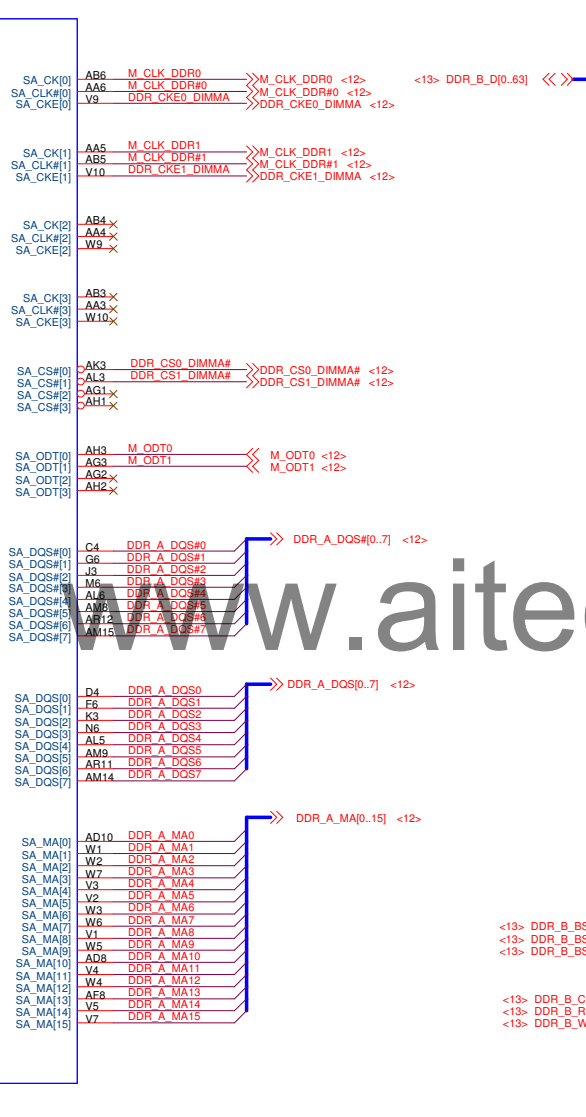
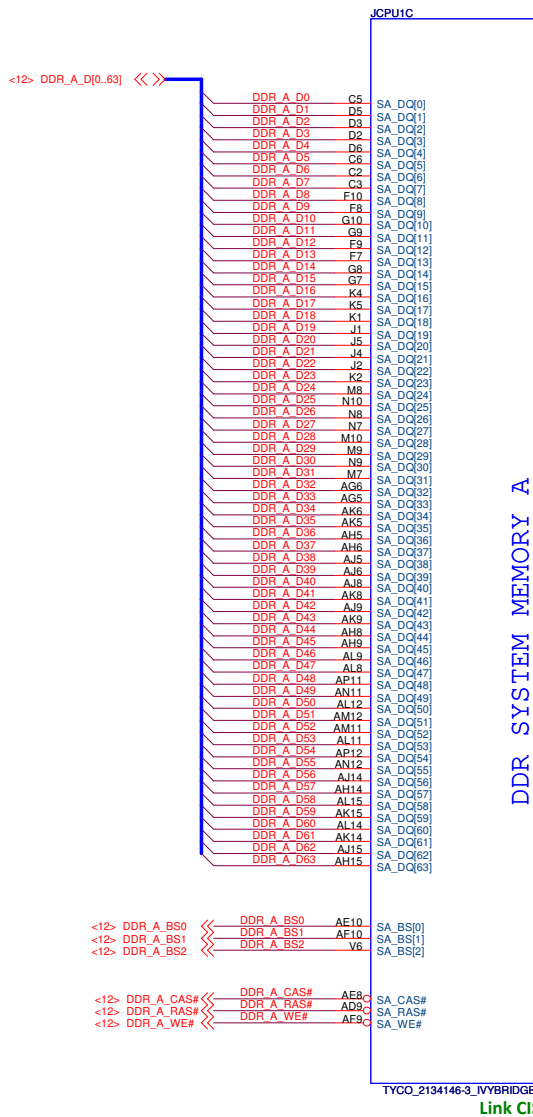
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Index and Config.			
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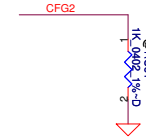
Ivy/Sandy Bridge (3/6)

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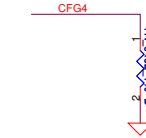
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CFG Straps for Processor



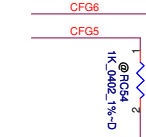
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed
------	---



Display Port Presence Strap

CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port
------	--



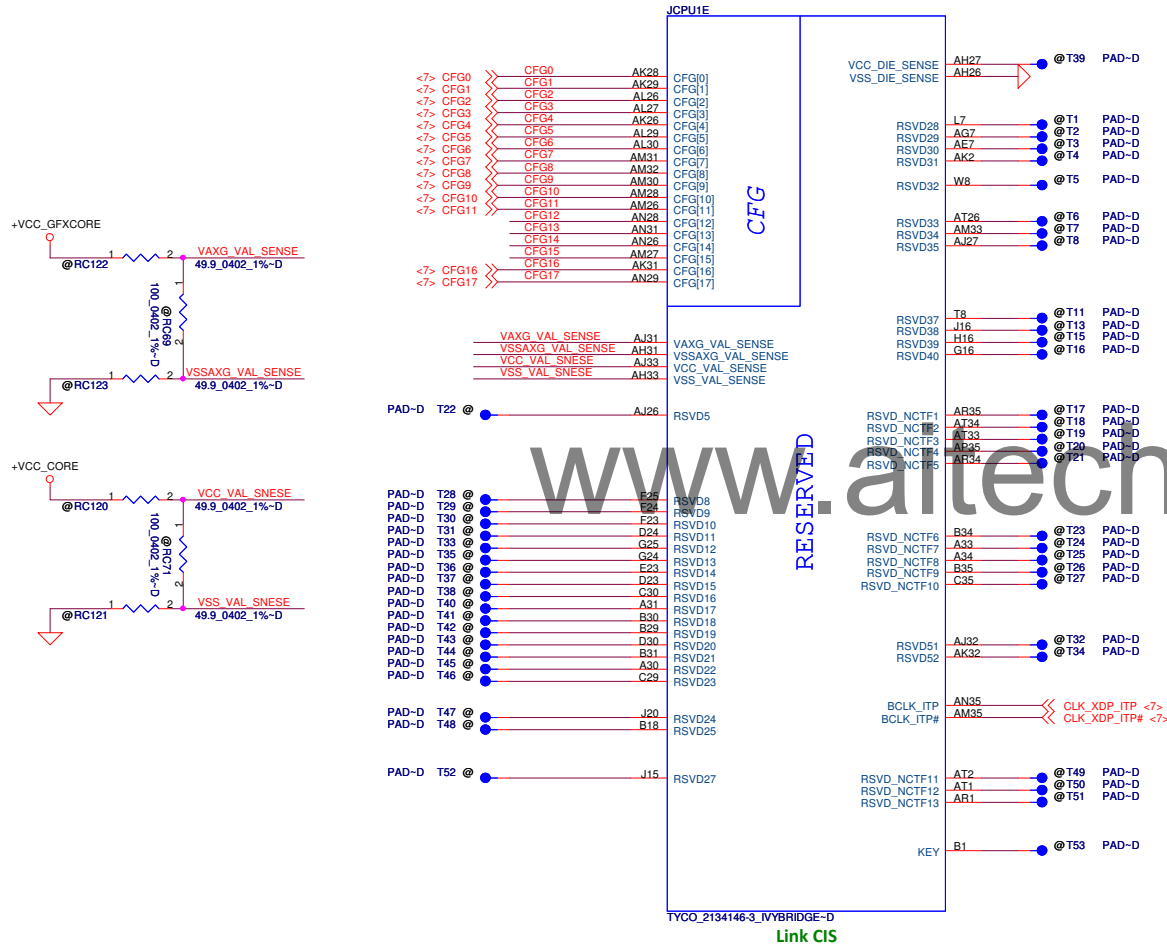
PCIe Port Bifurcation Straps

CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
----------	--



PEG DEFER TRAINING

CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training
------	---



TYCO_2134146-3_IVYBRIDGE-D
Link CIS

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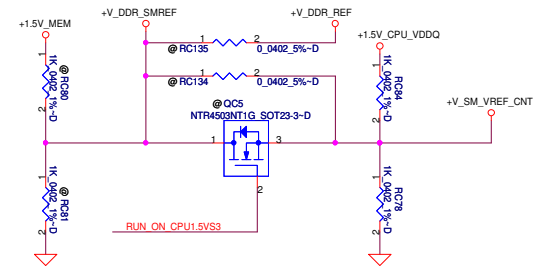
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Ivy/Sandy Bridge (4/6)

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[illegible]

POWER

GRAPHICS

MISC

SENSE LINES

VREF

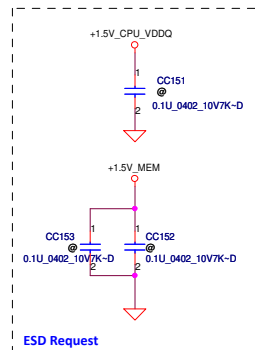
SA RAIL

DDR3 -1.5V RAILS

8V RAIL

ESD Request

Depop RC140 for ES2 CPU



JCPUH

AT36	VSS1	VSS81	AJ22
AT32	VSS2	VSS82	AJ18
AT29	VSS3	VSS83	AJ16
AT27	VSS4	VSS84	AJ13
AT25	VSS5	VSS85	AJ10
AT22	VSS6	A7	VSS86
AT19	VSS7	VSS87	AJ4
AT16	VSS8	VSS88	AJ3
AT13	VSS9	VSS89	AJ2
AT10	VSS10	VSS90	AJ1
AT7	VSS11	VSS91	AH25
AT4	VSS12	VSS92	AH24
AT3	VSS13	VSS93	AH23
AP25	VSS14	VSS94	AH20
AP22	VSS15	VSS95	AH25
AP19	VSS16	VSS96	AH28
AP17	VSS17	VSS98	AH26
AP13	VSS18	VSS99	AH22
AP10	VSS19	VSS100	AH19
AP7	VSS20	VSS101	AH16
AP4	VSS21	VSS102	AH7
AH2	VSS22	VSS103	AH4
AP34	VSS23	AC9	
AP31	VSS24	VSS104	AC8
AP28	VSS25	VSS105	AC7
AP25	VSS26	VSS106	A4
AP22	VSS27	VSS107	AF5
AP19	VSS28	VSS108	AF4
AP16	VSS29	VSS109	AF3
AP13	VSS30	VSS110	A2
AP10	VSS31	VSS111	A2
AP7	VSS32	VSS112	AE34
AP4	VSS33	VSS113	AE33
AP1	VSS34	VSS114	AE32
AN30	VSS35	VSS115	AE31
AN27	VSS36	VSS116	AE28
AN25	VSS37	VSS117	AE28
AN22	VSS38	VSS118	AE27
AN19	VSS39	VSS119	AE27
AN16	VSS40	VSS120	AE26
AN13	VSS41	VSS121	A07
AN10	VSS42	VSS122	A07
AN7	VSS43	VSS123	AC6
AN4	VSS44	VSS124	AC6
AN2	VSS45	VSS125	AC6
AN2	VSS46	VSS126	AC5
AM25	VSS47	VSS127	AC3
AM22	VSS48	VSS128	AC2
AM19	VSS49	VSS129	AB35
AM16	VSS50	VSS130	AB34
AM13	VSS51	VSS131	AB33
AM10	VSS52	VSS132	AB32
AM7	VSS53	VSS133	AB31
AM4	VSS54	VSS134	AB30
AM2	VSS55	VSS135	AB29
AM1	VSS56	VSS136	AB28
AL34	VSS57	VSS137	AB27
AL31	VSS58	VSS138	AB26
AL28	VSS59	VSS139	Y9
AL25	VSS60	VSS140	Y8
AL22	VSS61	VSS141	Y6
AL19	VSS62	VSS142	Y5
AL16	VSS63	VSS143	Y3
AL13	VSS64	VSS144	Y2
AL10	VSS65	VSS145	W35
AL7	VSS66	VSS146	W34
AL4	VSS67	VSS147	W33
AL2	VSS68	VSS148	W32
AK33	VSS69	VSS149	W31
AK30	VSS70	VSS150	W30
AK27	VSS71	VSS151	W29
AK25	VSS72	VSS152	W28
AK22	VSS73	VSS153	W26
AK19	VSS74	VSS154	W26
AK16	VSS75	VSS155	U8
AK13	VSS76	VSS156	U8
AK10	VSS77	VSS157	U6
VSS78	VSS78	VSS158	U8
AK4	VSS79	VSS159	U3
AJ25	VSS80	VSS160	U2

VSS

TYCO 21341-63 1VVBIDGE-D

1.0

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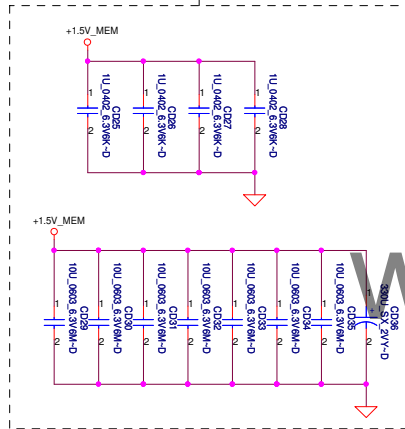
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 <8> DDR_B_DQ(0..63) <>>>
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 <8> DDR_B_MA(0..15) <>>>

All VREF traces should
 have 10 mil trace width

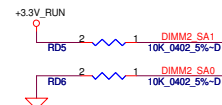
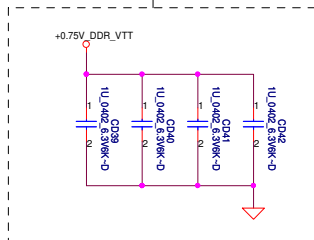


Populate RD4, De-Populate RD8 for Intel DDR3
 VREFDQ multiple methods M1
 Populate RD8, De-Populate RD4 for Intel DDR3
 VREFDQ multiple methods M3

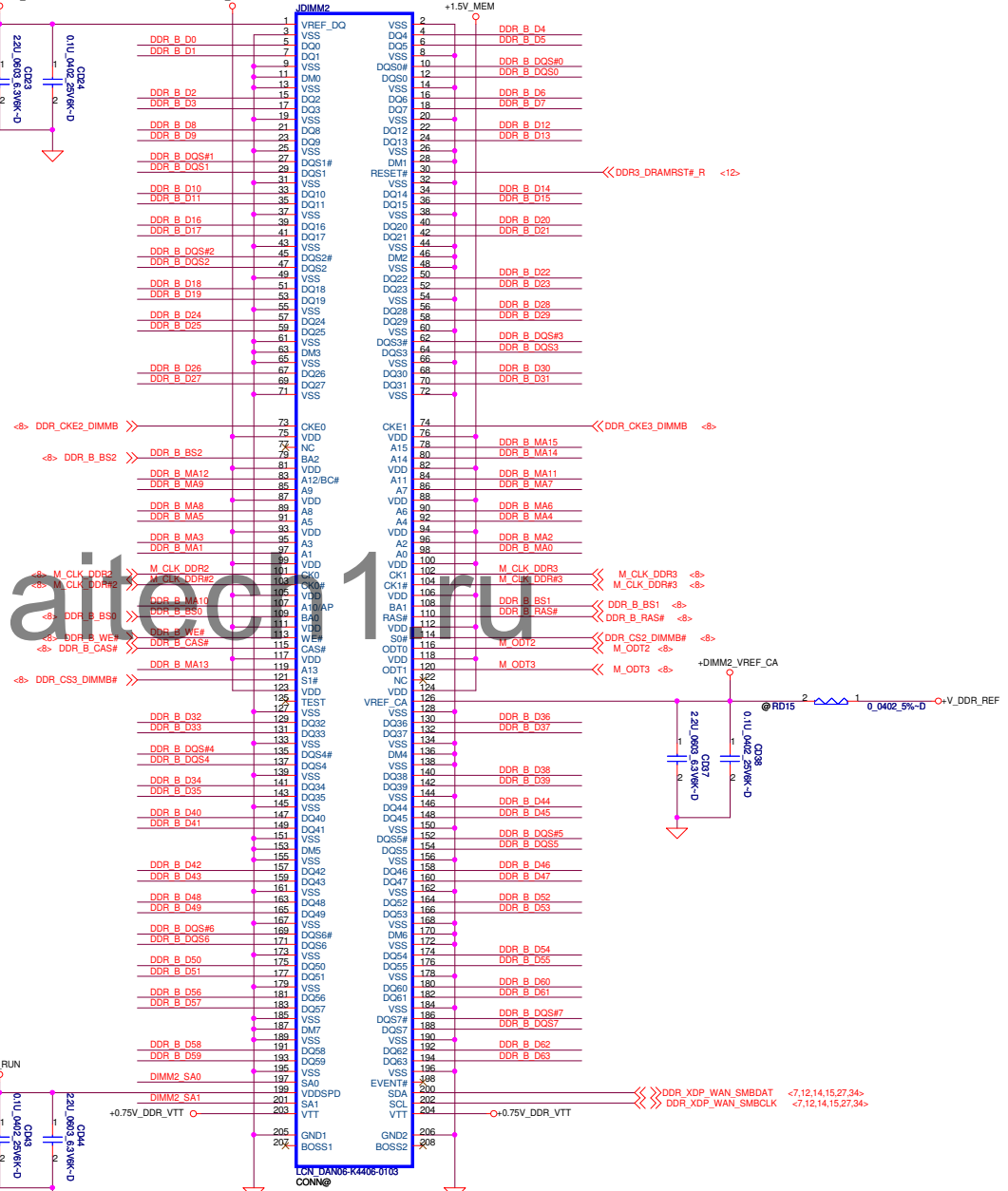
Layout Note:
 Place near JDIMM2



Layout Note:
 Place near JDIMM2.203,204



JDIMM2 Rev Type H=4 2-3A to 1 DIMMs/channel



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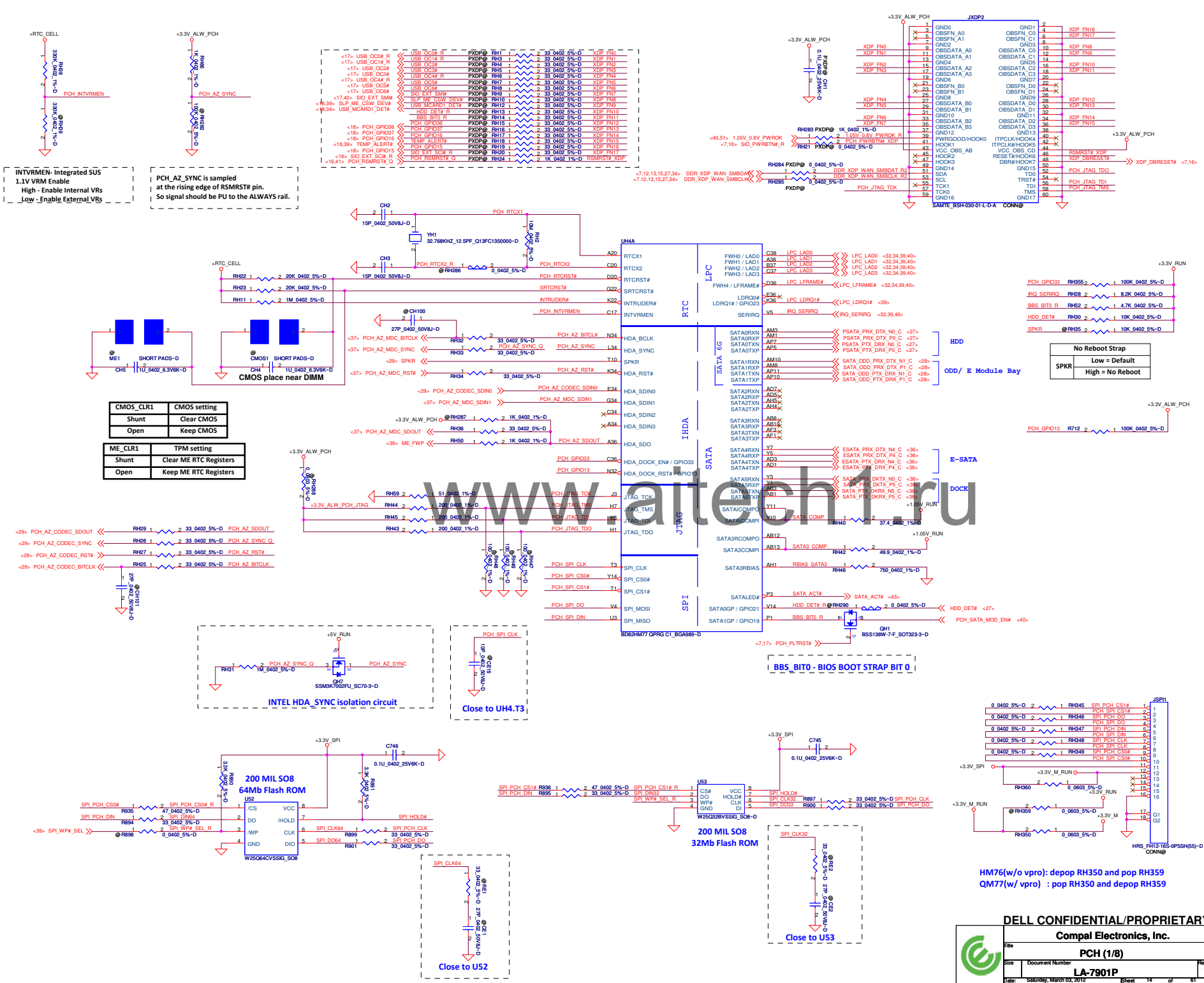
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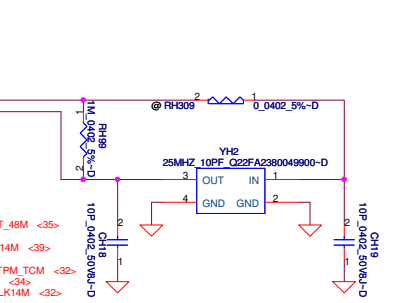
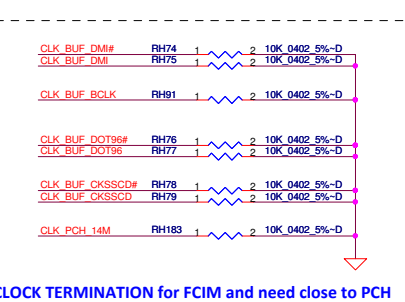
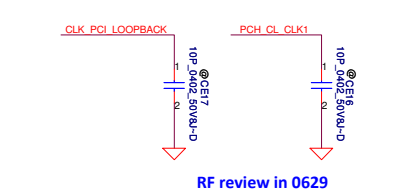
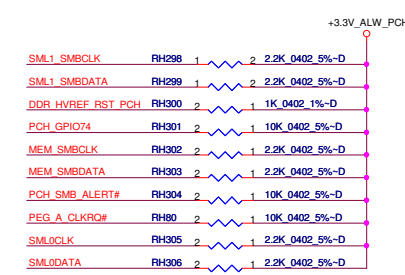
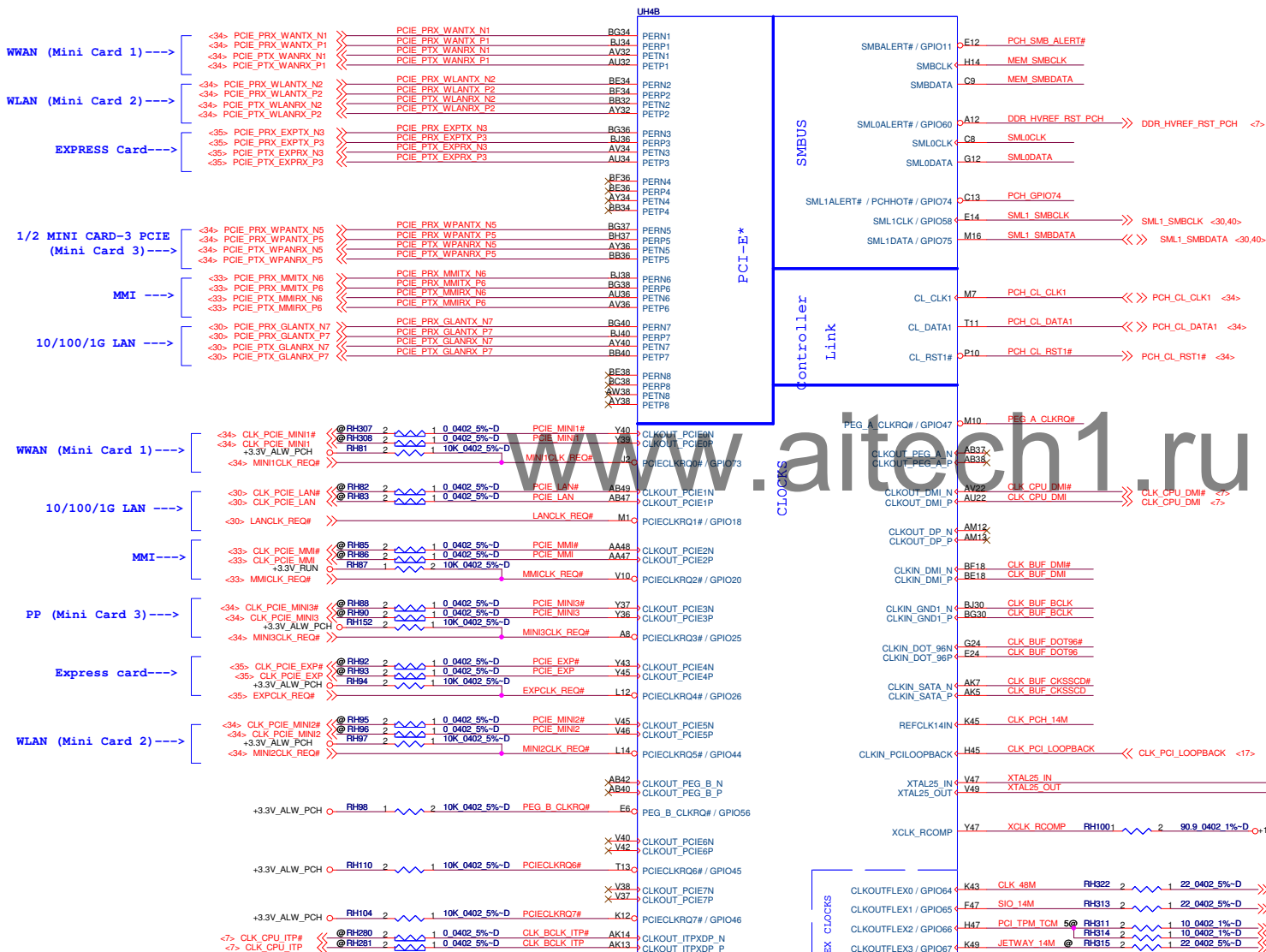
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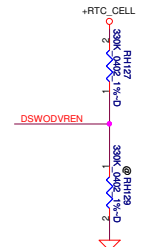
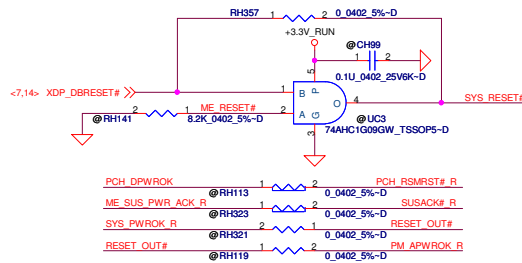
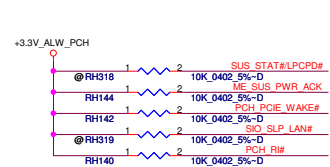
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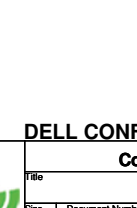
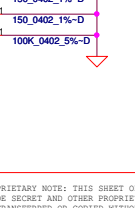
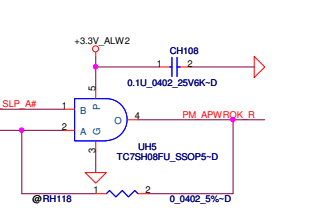
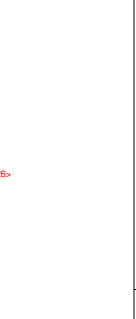
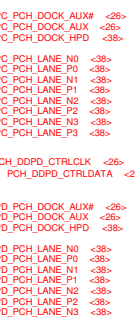
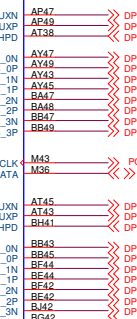
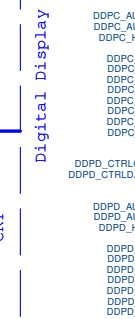
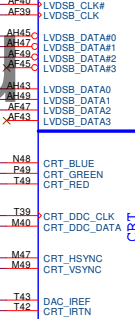
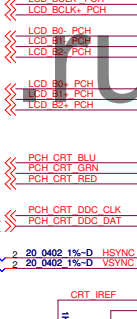
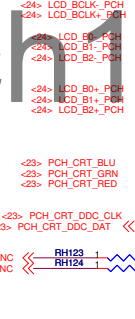
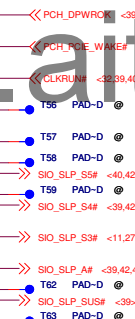
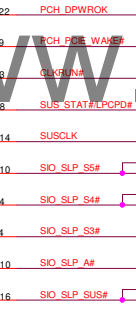
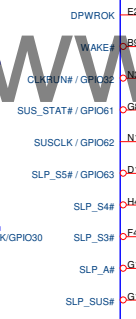
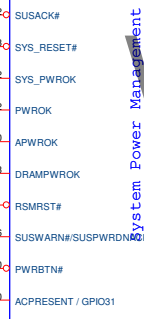
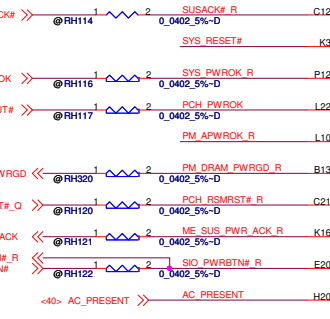
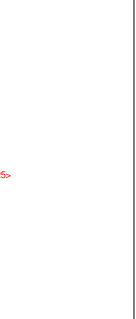
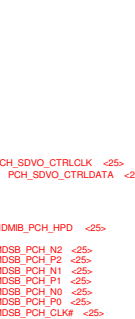
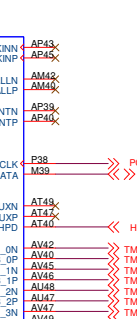
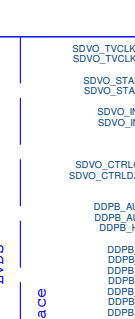
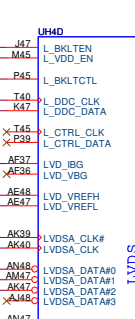
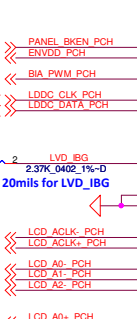
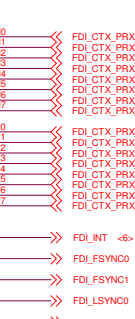
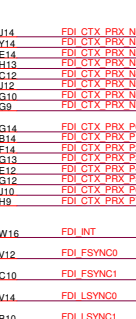
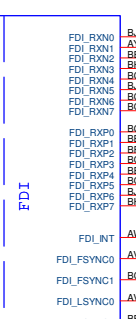
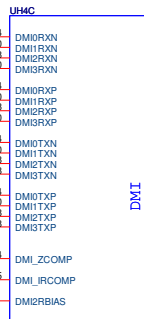
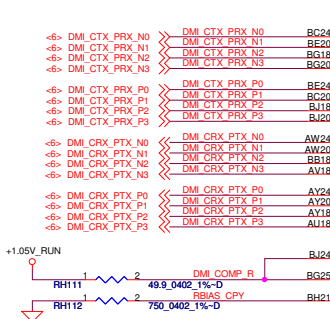
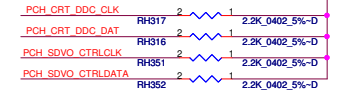




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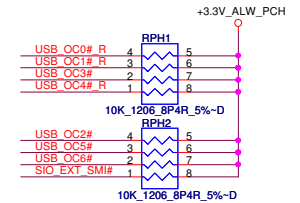
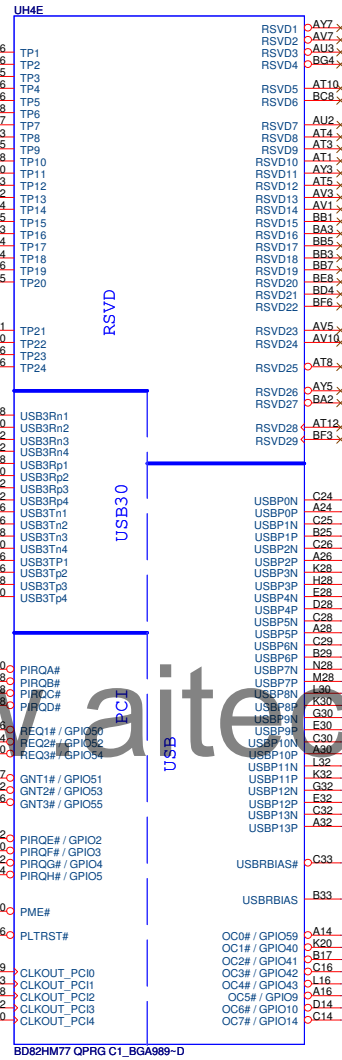
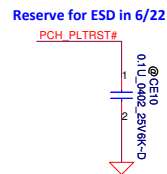
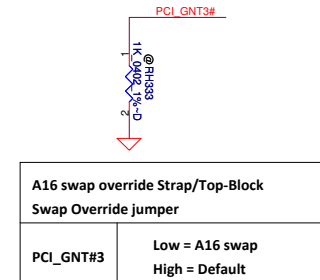
DSWODVREN - On Die DSW VR Enable
Enabled (DEFAULT)
HIGH: RH127 STUFFED, RH129 UNSTUFFED
Disabled
LOW: RH129 STUFFED, RH127 UNSTUFFED



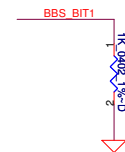
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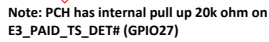
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Compal Electronics, Inc.
PCH (3/8)
LA-7901P
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Boot BIOS Strap		
BBS_BIT1	SATA_SLDP (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI





+3.3V_ALW_PCH

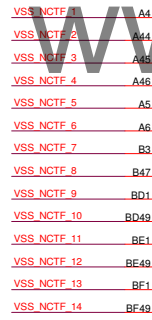
RH177 2 1 10K_0402 5%-D SIO EXT WAKE#

RH354 1 2 PCH GPIO15

RH179 2 1 1K_0402 1%-D PM LANPHY_ENABLE

RH180 2 1 10K_0402 5%-D PCH GPIO27

RH170 2 1 10K_0402 5%-D KB_DET#



GPIO

CPU/MISC

IP_ALERT#

NCTF

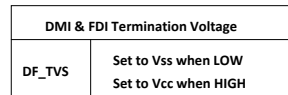
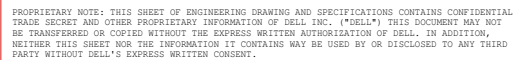


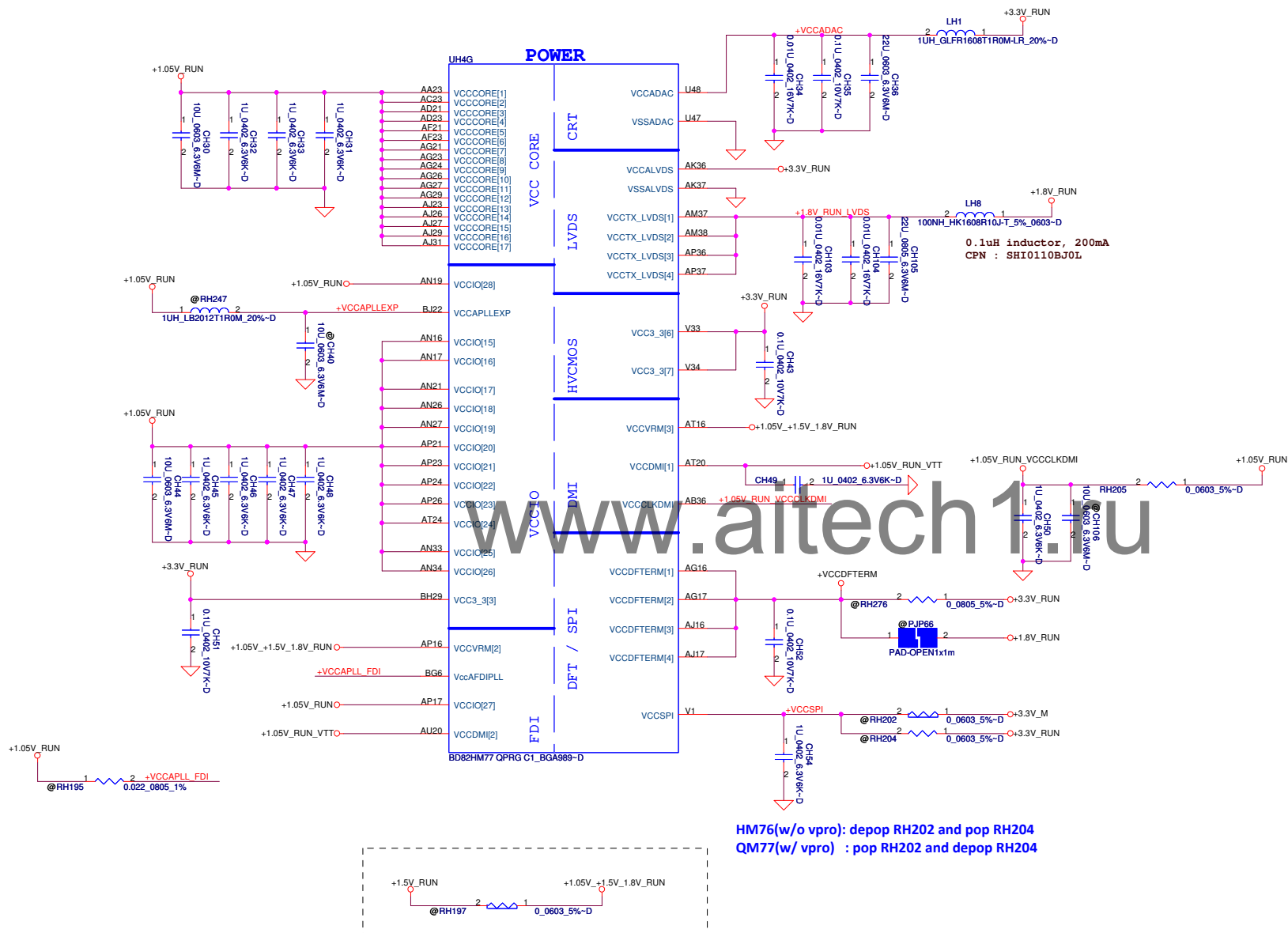
Diagram illustrating the placement of RH150 (CPU connector) near the branching point to the CPU and NVRAM connector.

The diagram shows a circuit layout with components labeled:

- +VCCDFTERM** (Power supply connection)
- 2.2K** (Resistor)
- 0.0402 5%-D** (Capacitor)
- RH149** (Component label)
- RH150** (Component label, indicated by a red arrow pointing to the junction)
- DF TVS** (TVS diode)
- 1K_0402 1%-D** (TVS diode)
- RH358** (Component label)
- 0.0402 5%-D** (Capacitor)
- H_SNB_IVB# <7#** (Signal line)

PLACE RH150 CLOSE TO THE BRANCHING POINT (TO CPU AND NVRAM CONNECTOR)

	TPM_ID0	TPM_ID1
China TPM	0	0
No TPM, No China TPM	0	1
TBD		
TPM	1	1



HM76(w/o vpro): depop RH202 and pop RH204
 QM77(w/ vpro) : pop RH202 and depop RH204

PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.288
VccADAC3	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.05	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW3_3	3.3	0.001
VCCDFTERM	1.8	0.002
VccRTC	3.3	6uA
VccSus3_3	3.3	0.126
VccSusHDA	3.3	0.01
VccVRM	1.8 / 1.5	0.167
VccClkDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

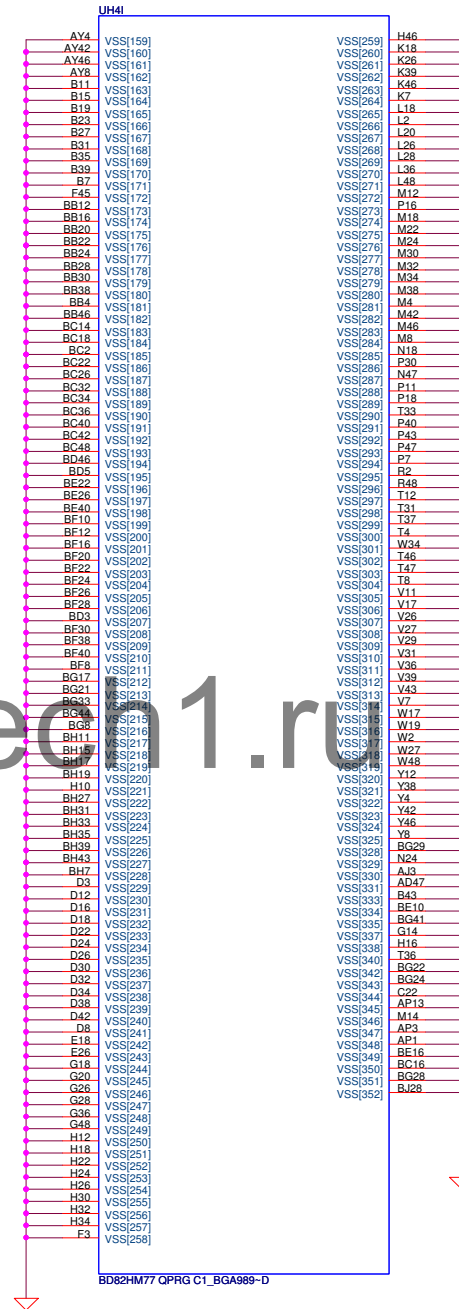
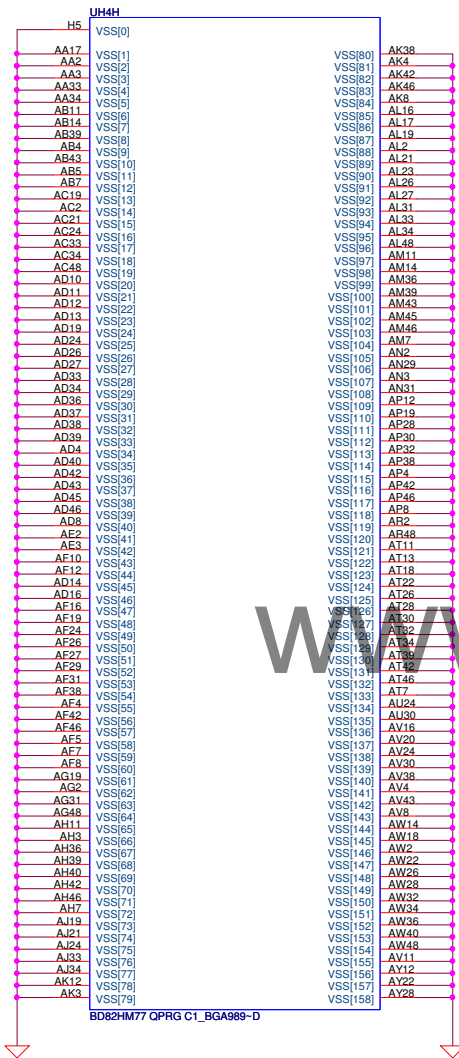
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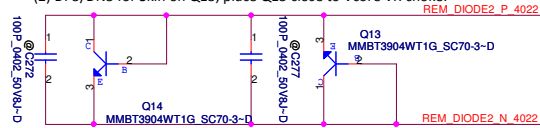


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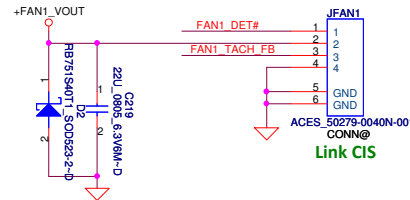
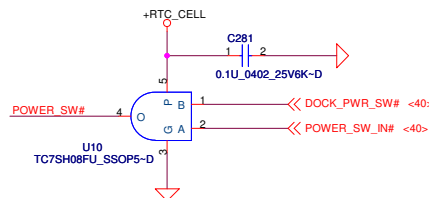
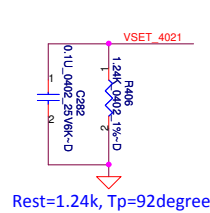
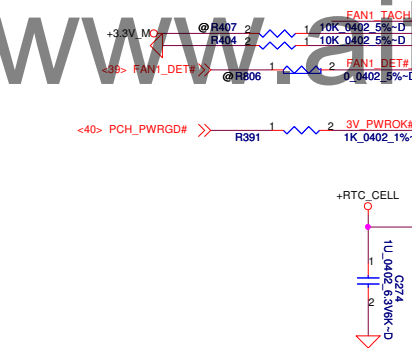
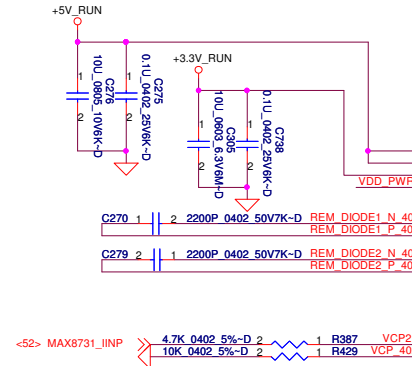
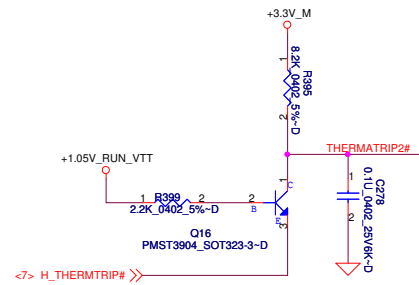
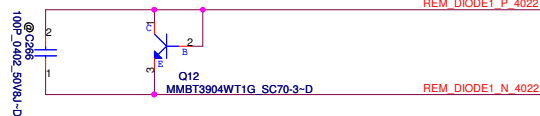
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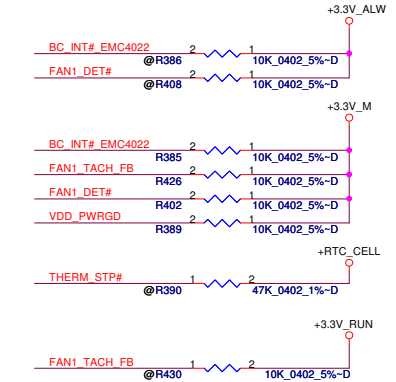
- (1) DP3/DN3 for SODIMM on Q14, place Q14 close to SODIMM and C272 close to Q14
- (2) DP5/DN5 for Skin on Q13, place Q13 close to Vcore VR choke.



Place under CPU
Place C266 close to the Q12 as possible



HM76(w/o vpro): depop R385 and pop R386
QM77(w/ vpro) : pop R385 and depop R386



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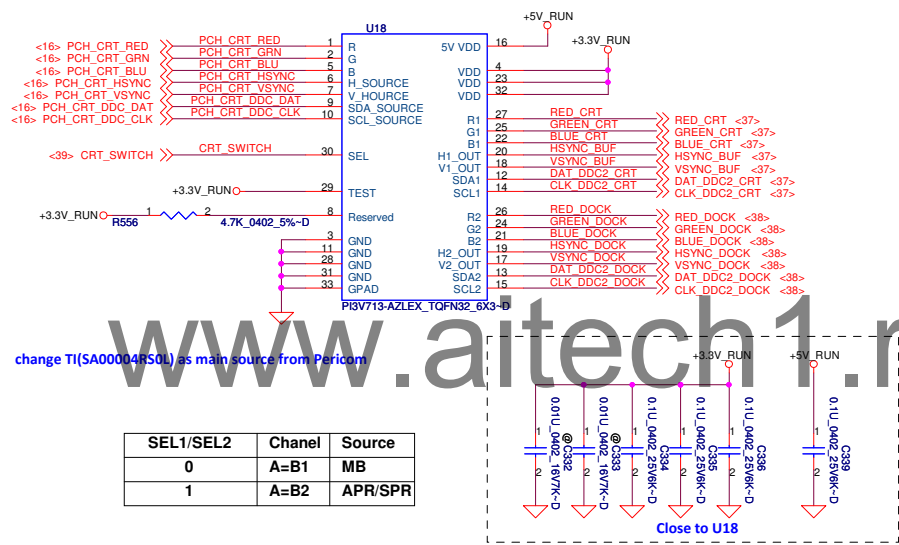
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FAN & Thermal Sensor			
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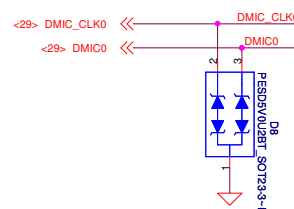
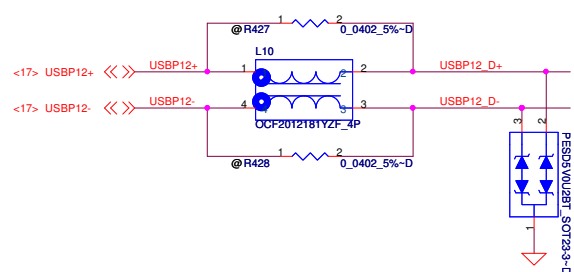
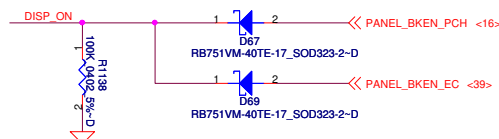
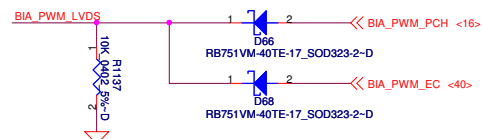
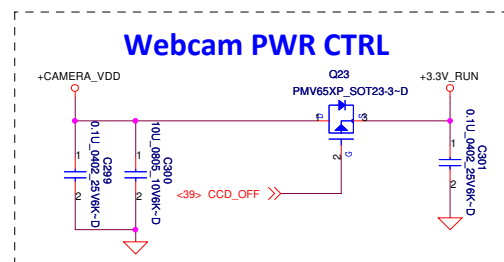
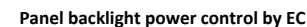
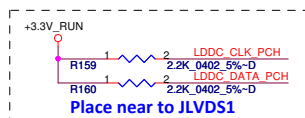
SW for MB/DOCK

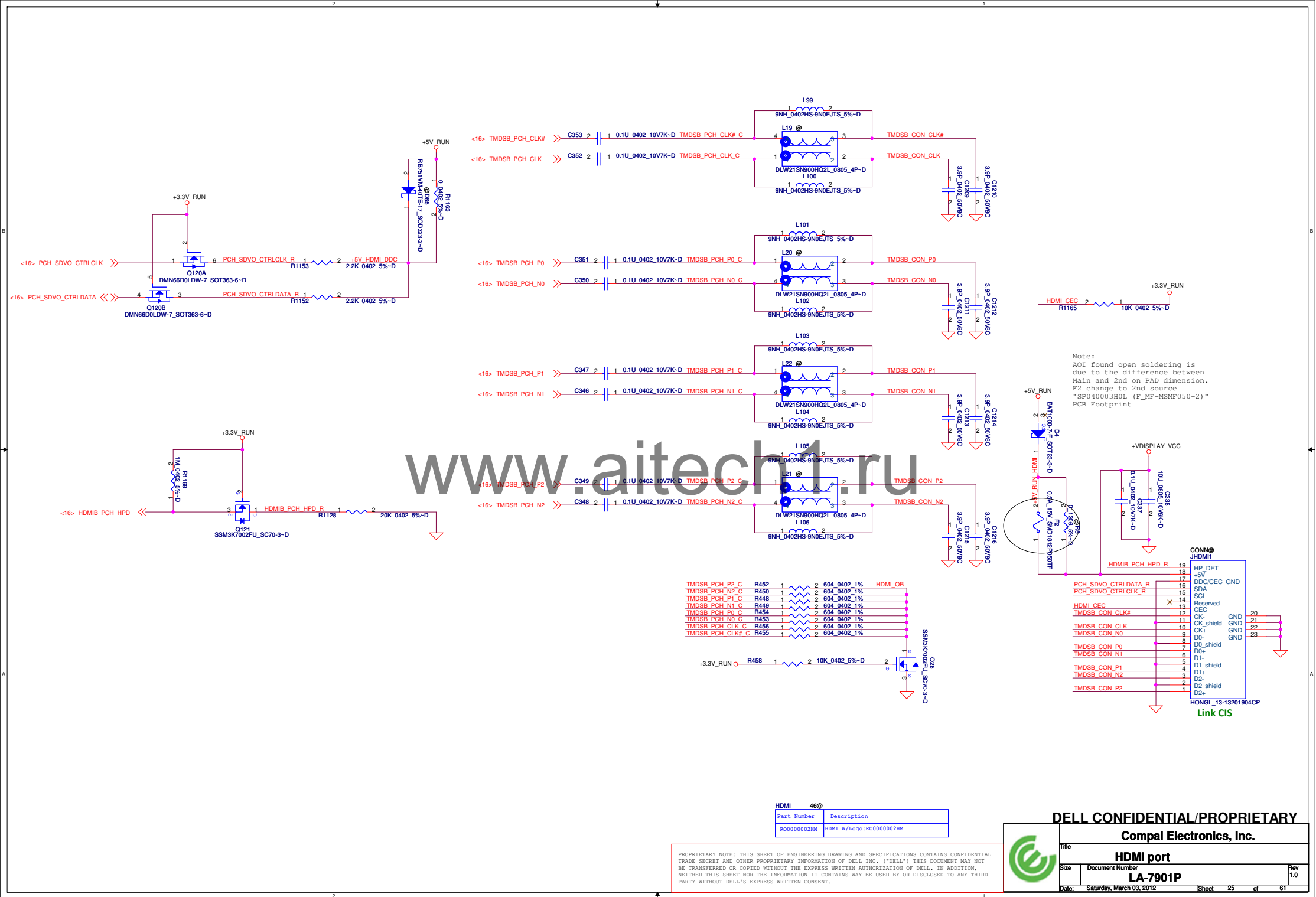


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Title		
CRT/Video switch		
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HDMI 46@	
Part Number	Description
R00000002HM	HDMI W/Logo:R00000002HM

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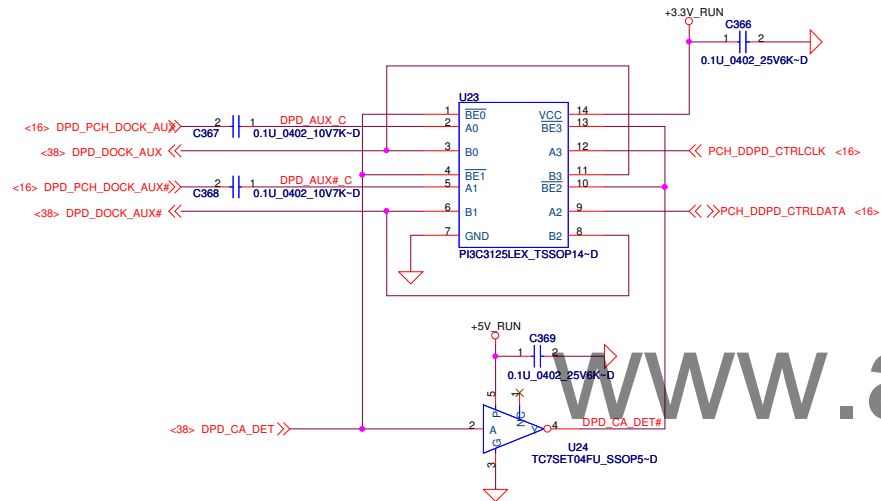
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HDMI port

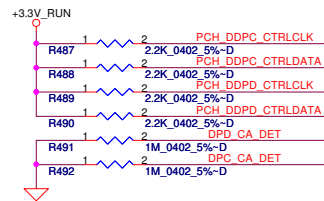
LA-7901P

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AUX/DDC SW for DPD to E-DOCK



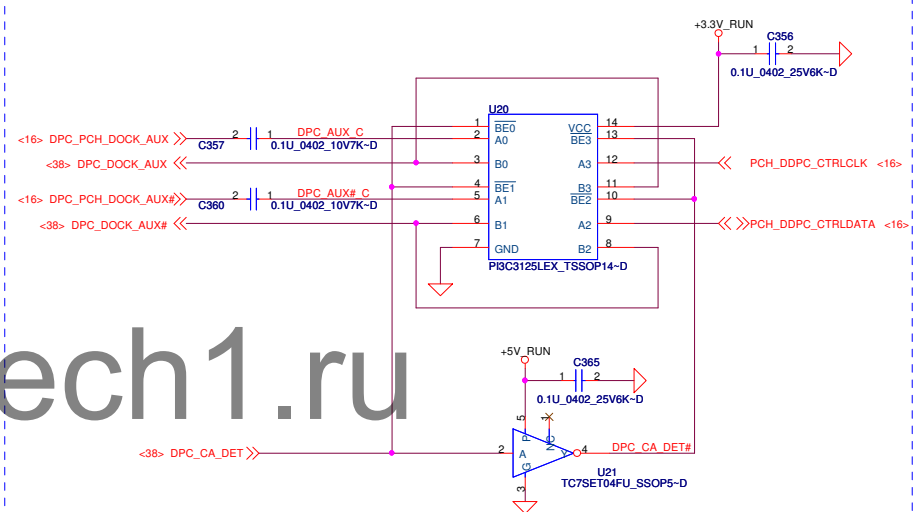
Note:When implement 2nd source, please check Vil and Vih spec is meet main source spec



Intel WW18 Strapping option

Intel WW18 Strapping option

AUX/DDC SW for DPC to E-DOCK



Note:When implement 2nd source, please check Vil and Vih spec is meet main source spec

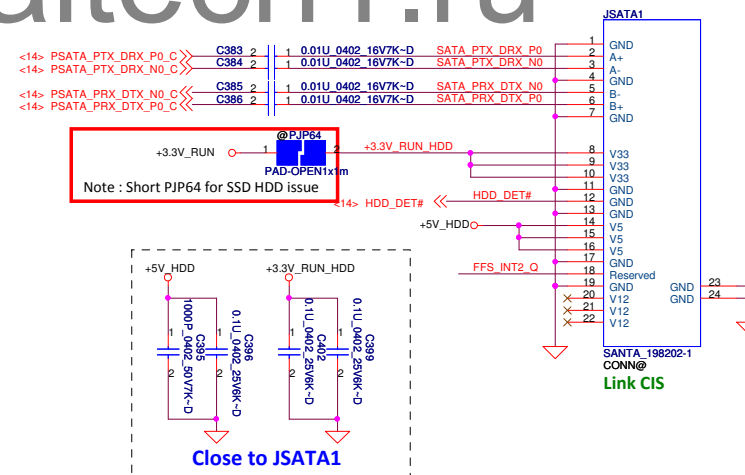
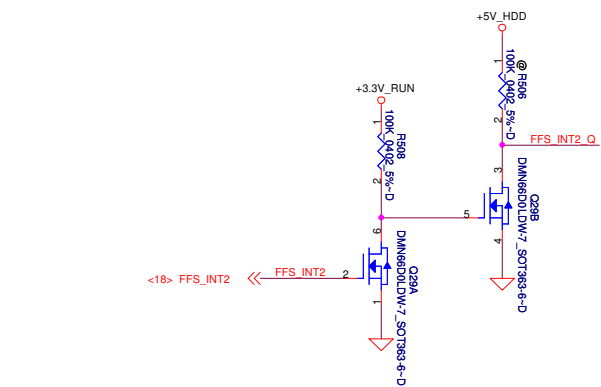
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Title		
DP SW		
Size	Document Number	Rev
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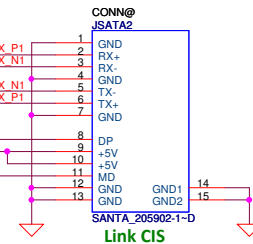
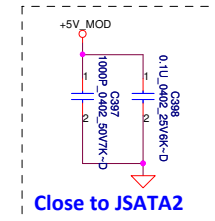
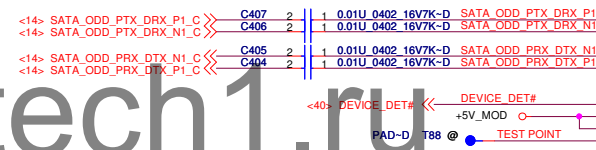
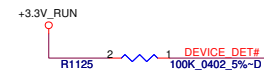
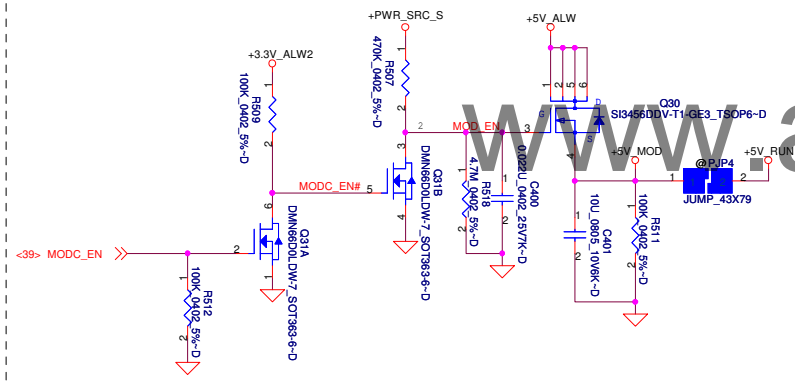
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ODD power



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15 mils trace

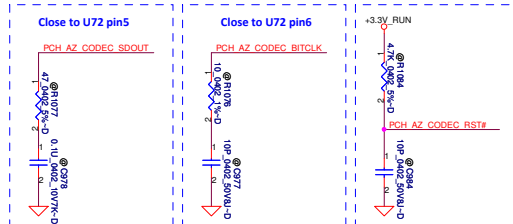
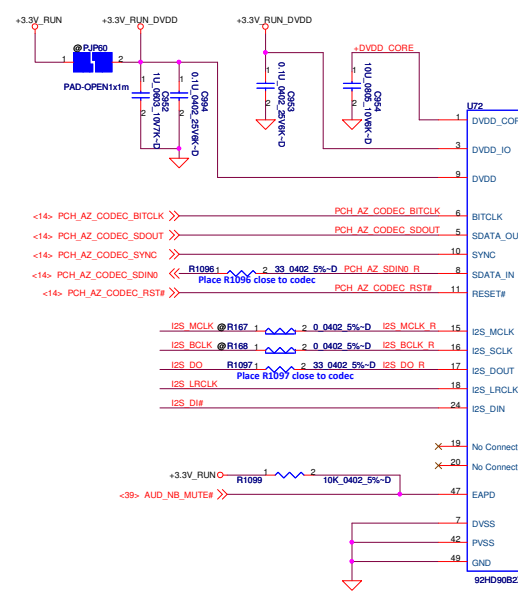
INT SPK L+
INT SPK R+
INT SPK L-
INT SPK R-

L91 1
L92 2
L93 3
L94 4

2 BLM18PG121SN1D 0603 INT SPK L+
2 BLM18PG121SN1D 0603 INT SPK R+
2 BLM18PG121SN1D 0603 INT SPK L-
2 BLM18PG121SN1D 0603 INT SPK R-

C97 2200p 500V7K-D
C98 2200p 500V7K-D
C99 2200p 500V7K-D

R10 3.3 500V7K-D
R11 3.3 500V7K-D
R12 3.3 500V7K-D
R13 3.3 500V7K-D
R14 3.3 500V7K-D
R15 3.3 500V7K-D
R16 3.3 500V7K-D
R17 3.3 500V7K-D
R18 3.3 500V7K-D
R19 3.3 500V7K-D
R20 3.3 500V7K-D
R21 3.3 500V7K-D
R22 3.3 500V7K-D
R23 3.3 500V7K-D
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R86 3.3 500V7K-D
R87 3.3 500V7K-D
R88 3.3 500V7K-D
R89 3.3 500V7K-D
R90 3.3 500V7K-D
R91 3.3 500V7K-D
R92 3.3 500V7K-D
R93 3.3 500V7K-D
R94 3.3 500V7K-D
R95 3.3 500V7K-D
R96 3.3 500V7K-D
R97 3.3 500V7K-D
R98 3.3 500V7K-D
R99 3.3 500V7K-D
R100 3.3 500V7K-D
R101 3.3 500V7K-D
R102 3.3 500V7K-D
R103 3.3 500V7K-D
R104 3.3 500V7K-D
R105 3.3 500V7K-D
R106 3.3 500V7K-D
R107 3.3 500V7K-D
R108 3.3 500V7K-D
R109 3.3 500V7K-D
R110 3.3 500V7K-D
R111 3.3 500V7K-D
R112 3.3 500V7K-D
R113 3.3 500V7K-D
R114 3.3 500V7K-D
R115 3.3 500V7K-D
R116 3.3 500V7K-D
R117 3.3 500V7K-D
R118 3.3 500V7K-D
R119 3.3 500V7K-D
R120 3.3 500V7K-D
R121 3.3 500V7K-D
R122 3.3 500V7K-D
R123 3.3 500V7K-D
R124 3.3 500V7K-D
R125 3.3 500V7K-D
R126 3.3 500V7K-D
R127 3.3 500V7K-D
R128 3.3 500V7K-D
R129 3.3 500V7K-D
R130 3.3 500V7K-D
R131 3.3 500V7K-D
R132 3.3 500V7K-D
R133 3.3 500V7K-D
R134 3.3 500V7K-D
R135 3.3 500V7K-D
R136 3.3 500V7K-D
R137 3.3 500V7K-D
R138 3.3 500V7K-D
R139 3.3 500V7K-D
R140 3.3 500V7K-D
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R142 3.3 500V7K-D
R143 3.3 500V7K-D
R144 3.3 500V7K-D
R145 3.3 500V7K-D
R146 3.3 500V7K-D
R147 3.3 500V7K-D
R148 3.3 500V7K-D
R149 3.3 500V7K-D
R150 3.3 500V7K-D
R151 3.3 500V7K-D
R152 3.3 500V7K-D
R153 3.3 500V7K-D
R154 3.3 500V7K-D
R155 3.3 500V7K-D
R156 3.3 500V7K-D
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R177 3.3 500V7K-D
R178 3.3 500V7K-D
R179 3.3 500V7K-D
R180 3.3 500V7K-D
R181 3.3 500V7K-D
R182 3.3 500V7K-D
R183 3.3 500V7K-D
R184 3.3 500V7K-D
R185 3.3 500V7K-D
R186 3.3 500V7K-D
R187 3.3 500V7K-D
R188 3.3 500V7K-D
R189 3.3 500V7K-D
R190 3.3 500V7K-D
R191 3.3 500V7K-D
R192 3.3 500V7K-D
R193 3.3 500V7K-D
R194 3.3 500V7K-D
R195 3.3 500V7K-D
R196 3.3 500V7K-D
R197 3.3 500V7K-D
R198 3.3 500V7K-D
R199 3.3 500V7K-D
R200 3.3 500V7K-D
R201 3.3 500V7K-D
R202 3.3 500V7K-D
R203 3.3 500V7K-D
R204 3.3 500V7K-D
R205 3.3 500V7K-D
R206 3.3 500V7K-D
R207 3.3 500V7K-D
R208 3.3 500V7K-D
R209 3.3 500V7K-D
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R211 3.3 500V7K-D
R212 3.3 500V7K-D
R213 3.3 500V7K-D
R214 3.3 500V7K-D
R215 3.3 500V7K-D
R216 3.3 500V7K-D
R217 3.3 500V7K-D
R218 3.3 500V7K-D
R



The schematic diagram illustrates the HP sense circuit for the DMN66D0LDW-7. Key components and connections include:

- Power Supply:** A 3.3V_VIN supply is connected to the circuit.
- Resistors:**
 - R1087 (100k) is connected between 3.3V_VIN and the gate of MOSFET Q107A.
 - R1088 (20k) is connected between the gate of MOSFET Q107A and the gate of MOSFET Q107B.
- Capacitors:**
 - C880 (0.1uF) is connected between the 3.3V_VIN supply and ground.
 - C887 (0.1uF) is connected between the drain of MOSFET Q107B and ground.
- MOSFETs:**
 - Q107A (DMN66D0LDW-7) is an N-channel MOSFET with its gate connected to the 3.3V_VIN supply through R1087 and its drain connected to the drain of Q107B.
 - Q107B (DMN66D0LDW-7) is an N-channel MOSFET with its gate connected to the gate of Q107A through R1088 and its drain connected to the drain of Q107A.
- Output:** The output of the circuit is labeled AUD_HP_NB_SENSE, which is connected to the drain of MOSFET Q107B.


[illegible]

place at AGND and DGND plane

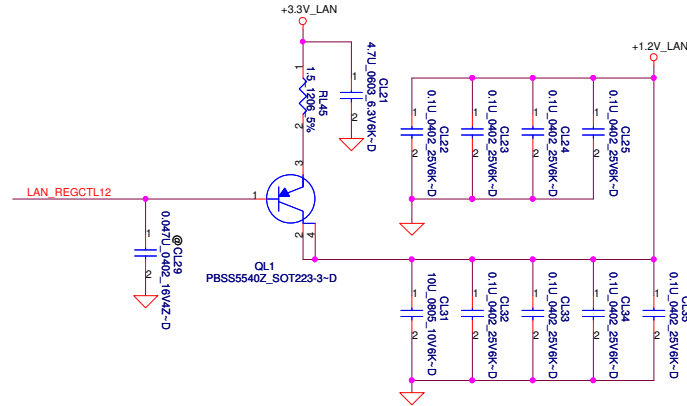
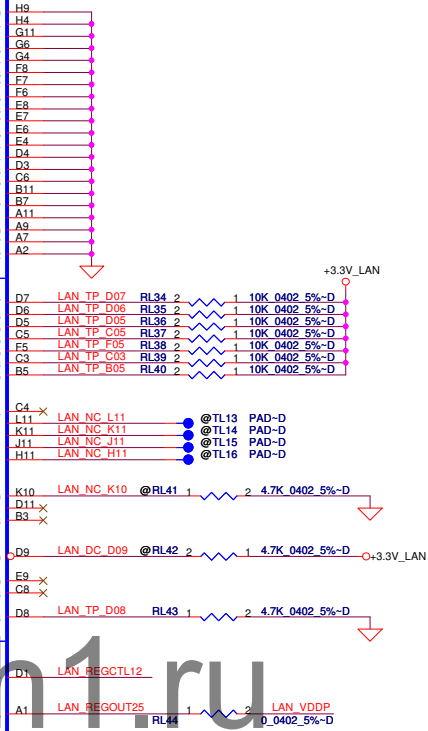
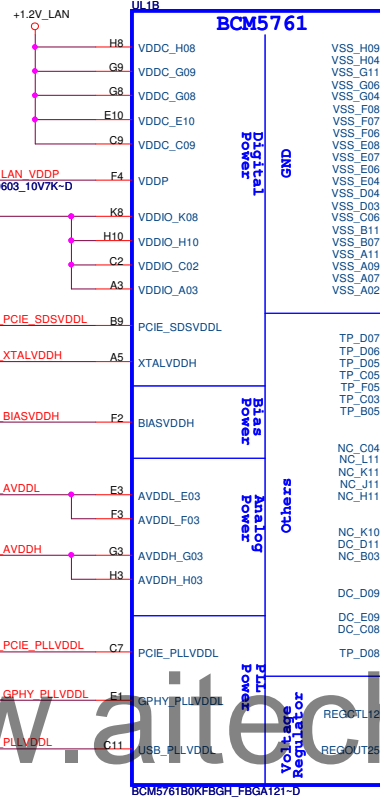
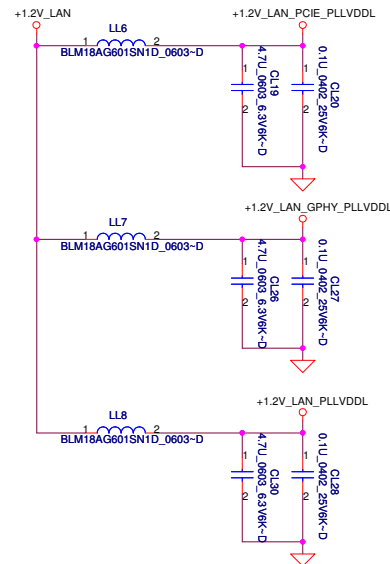
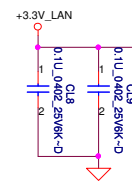
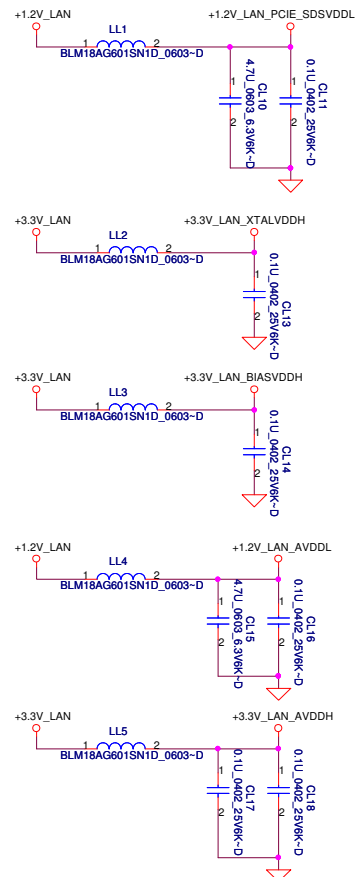
Resistor	SENSE_A	SENSE_B
39.2K	PORT A	PORT E
20K	PORT B	PORT F
10K	NA	DMIC0
5.11K	SPDIFOUT0	SPDIFOUT1 (DMIC1)
2.49K	Pull-up to AVDD	

The timing diagram shows the following signals and components:

- DAI_BCLK#**: Signal 1, 22.0402 5%-D, 1A, 1Y#
- DAI_LRCLK#**: Signal 2, 0.0402 5%-D, 2A, 2Y#
- DAI_DO#**: Signal 3, 0.0402 5%-D, 3A, 3Y#
- DAI_12MHz#**: Signal 4, 22.0402 5%-D, 4A, 4Y#
- DAI_DI#**: Signal 5, 0.0402 5%-D, 5A, 5Y#
- DAI_DIF#**: Signal 6, 0.0402 1%-D, 6A, 6Y#
- EN I2S_NB CODEC#**: Signal 7, 1K_0402_1%-D, 7A, 7Y#
- OE#**: Signal 8, 0.0402 1%-D, 8A, 8Y#
- CD74HC366M96**: Component 1, 16 pins, 16Y#
- D58**: Component 2, 16 pins, 16Y#
- 3.3V RUN**: Power supply

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	Title		
	Azalia (HD) Codec		
	Size	Document Number	Rev
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Size

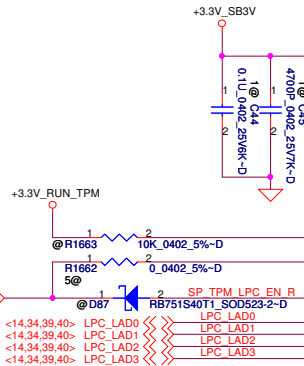
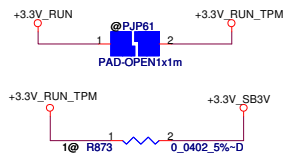
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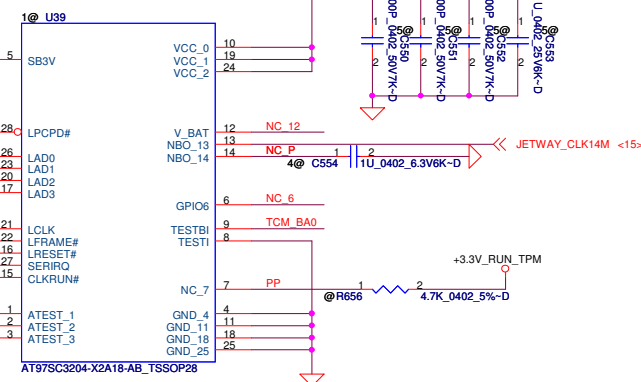
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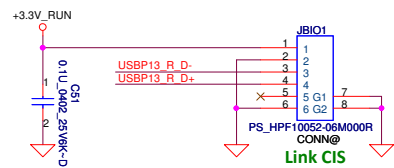
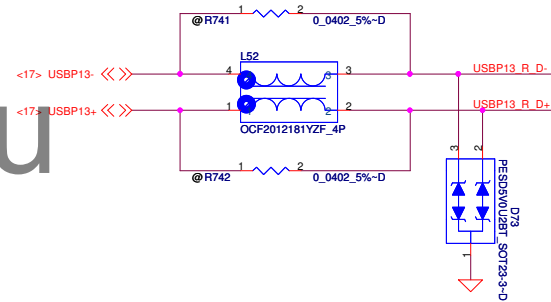
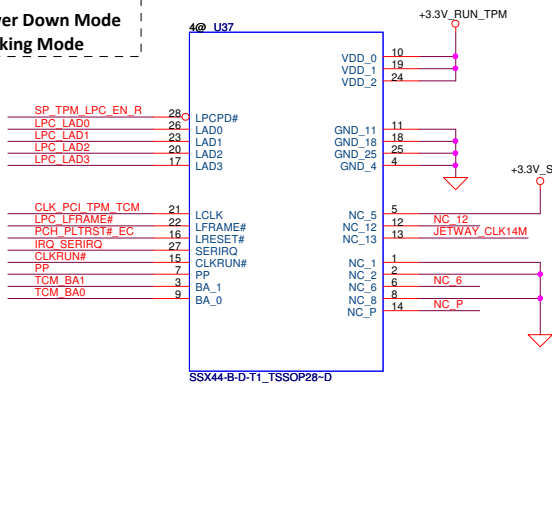
ATME1 TPM for E4



Co-lay U37 and U39
LPC layout: Place TCM first and then end LPC with TPM.

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China TCM: NationZ & Jetway co-lay

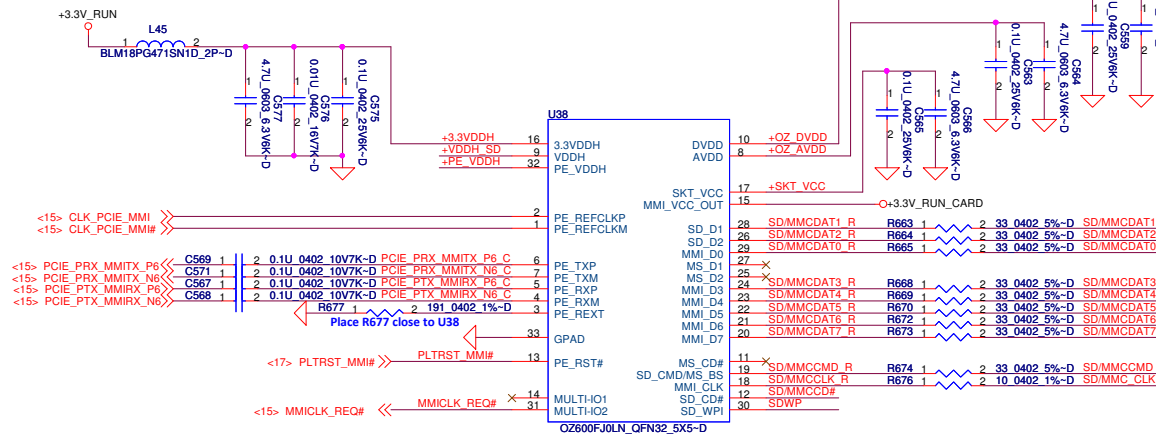
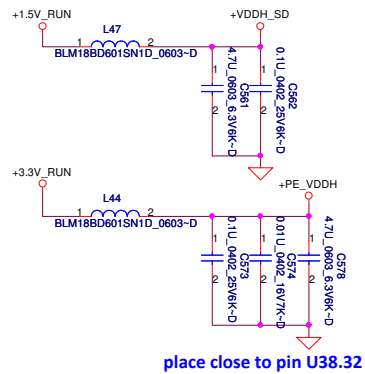
LOW:Power Down Mode
High:Working Mode



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TPM/TCM/BIO Conn	
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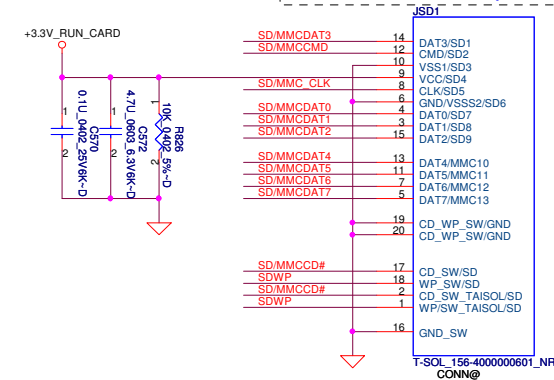
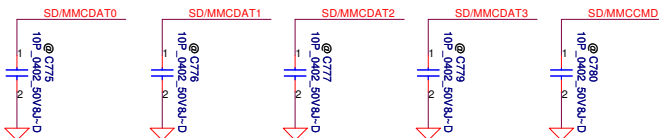
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Note: The trace need to route as daisy-chain and the trace of SD signals need to route as short as possible

Vendor review in 6/22 and reserve for SD3.0 UHS-I 200MHz transfer



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Card Reader OZ600FJ0

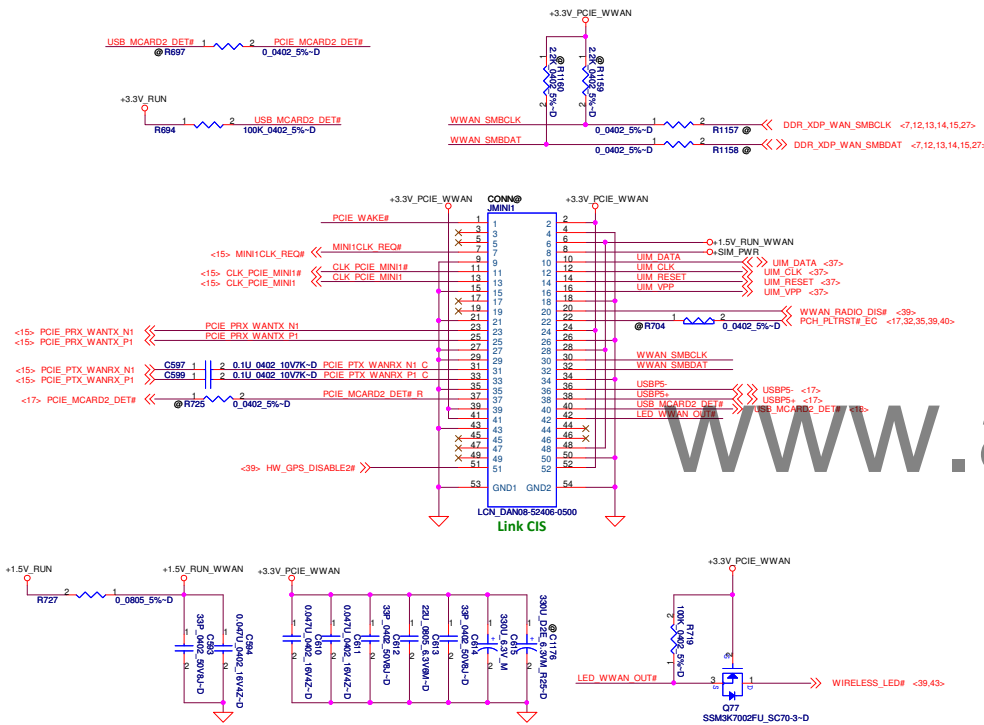
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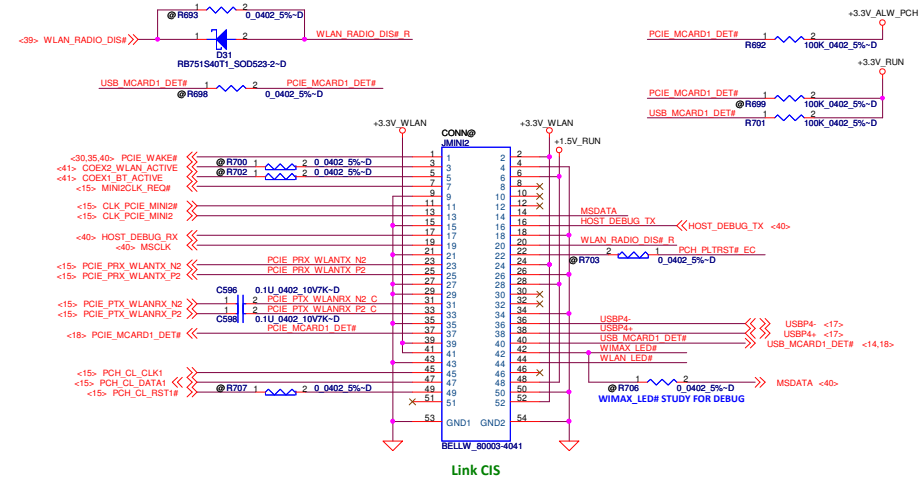
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Mini WWAN/GPS/LTE/UWB H=4

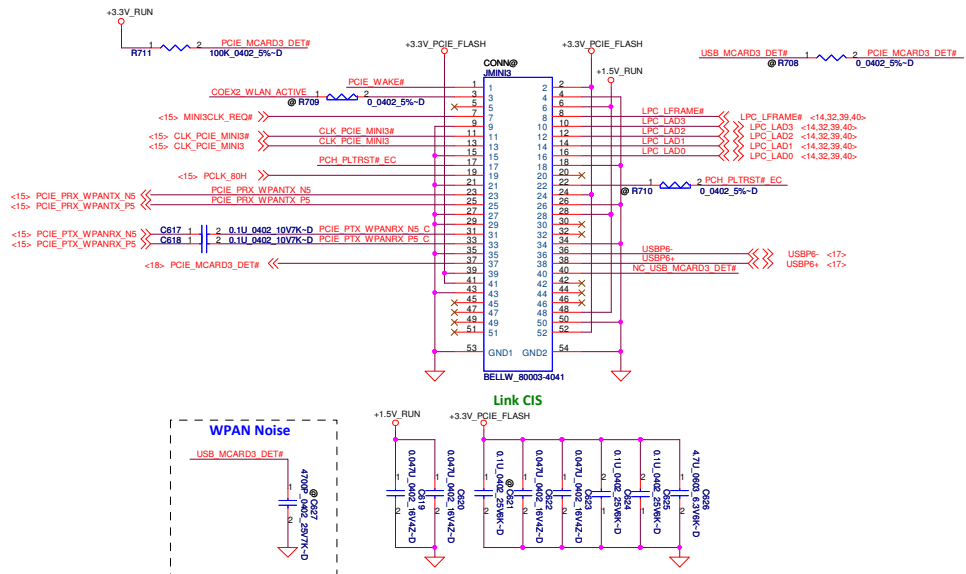


PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+9%	1000	750	
+3.3Vaux	+9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+5%	500	375	NA

Mini WLAN/WIMAX H=6.7



1/2 Minicard Pink Pather/60GHz Card H=6.7



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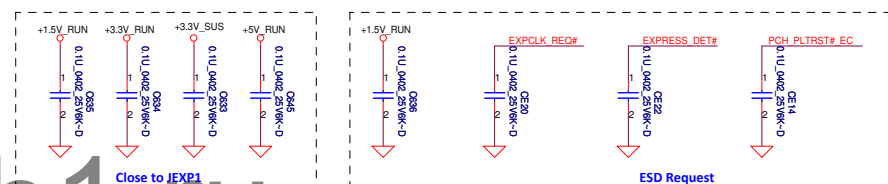
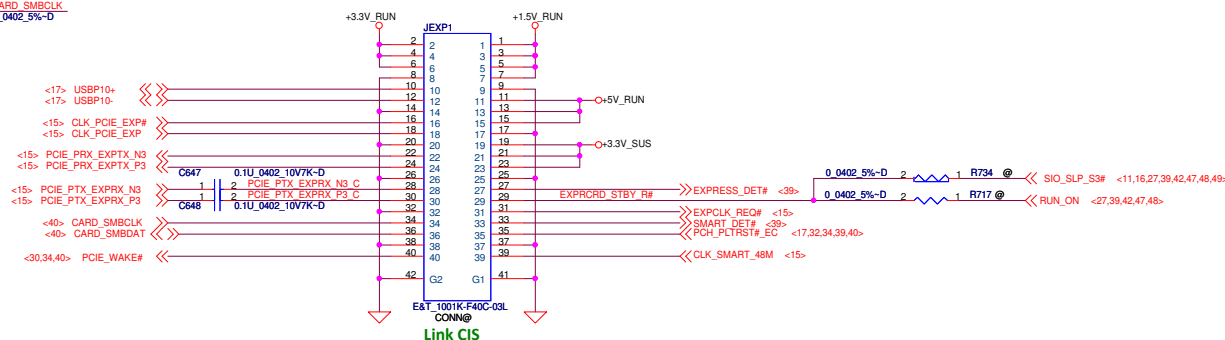
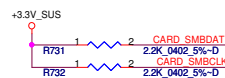
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Mini Card

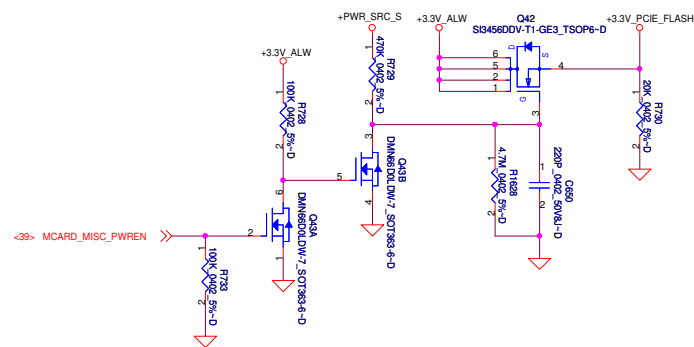
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Express/Smart Card Conn.



Power Control for Mini card3



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MINI CARD PWR/EXP SC

LA-7901P

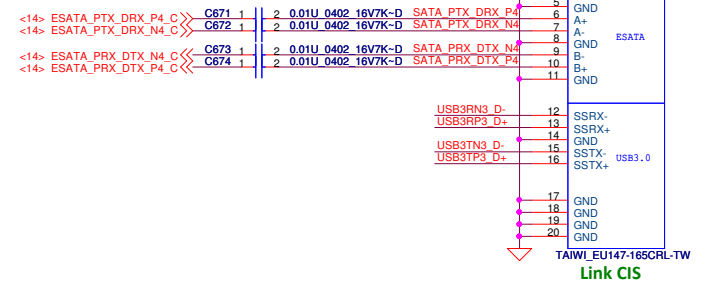
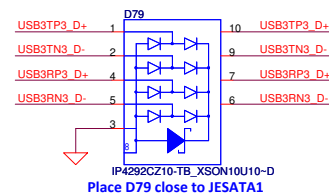
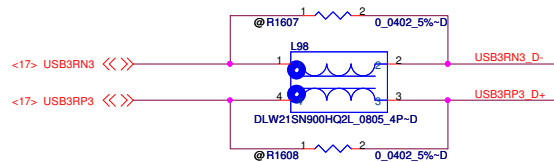
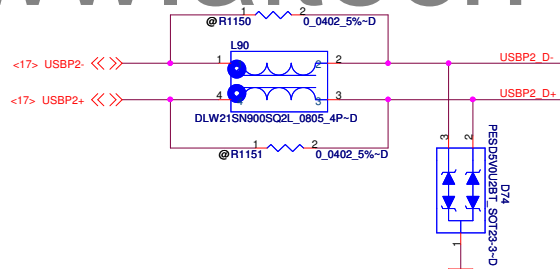
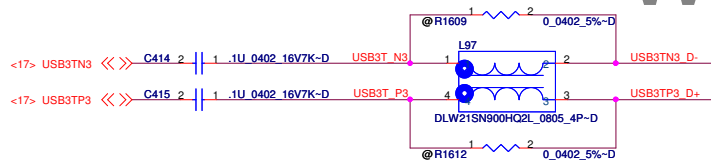
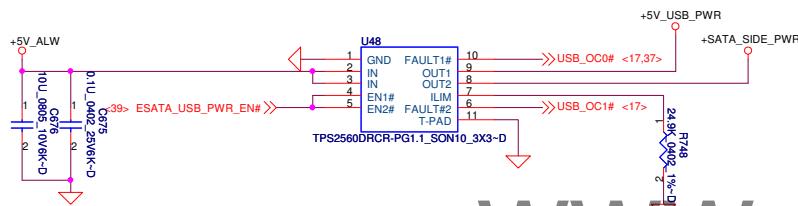
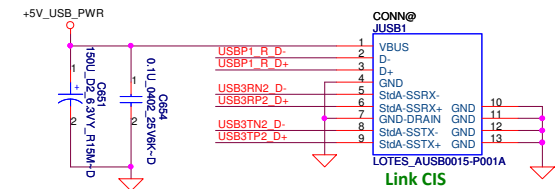
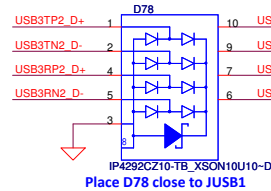
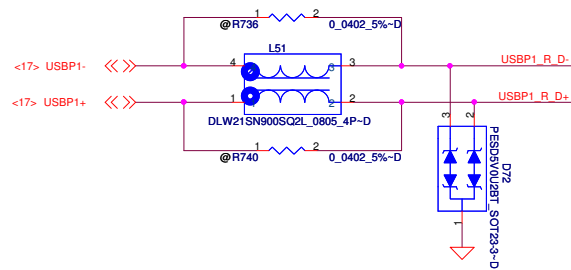
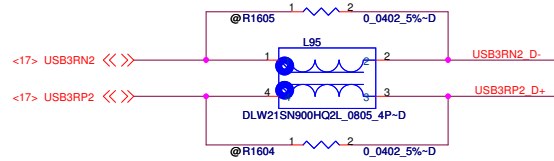
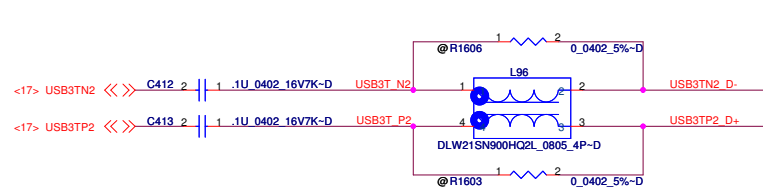
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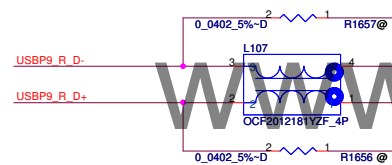
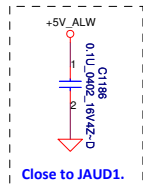
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Pin connection diagram for the Link C1S module. The diagram shows a 22-pin connector on the left, labeled 'JAUD1' and 'CONN@'. The pins are numbered 1 through 22. On the right, the corresponding signals are listed:

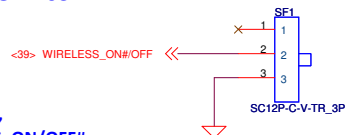
- Pin 1: AUD_HP_OUT_R <29>
- Pin 2: AUD_HP_OUT_L <29>
- Pin 3: MIC_IN_R <29>
- Pin 4: MIC_IN_L <29>
- Pin 5: AUD_HP_NB_SENSE <29,39>
- Pin 6: USB_OC4# <17>
- Pin 7: USB_S1DC_EN# <39>
- Pin 8: +5V_ALW
- Pin 9: USBP9_R D+
- Pin 10: USBP9_R D-
- Pin 11: GND
- Pin 12: GND
- Pin 13: GND
- Pin 14: GND
- Pin 15: GND
- Pin 16: GND
- Pin 17: GND
- Pin 18: GND
- Pin 19: GND
- Pin 20: GND
- Pin 21: GND
- Pin 22: GND

The diagram also shows a power supply connection for +5V_ALW and a ground connection for GND.

Link CIS



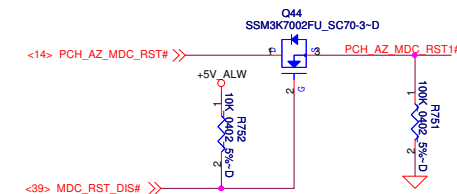
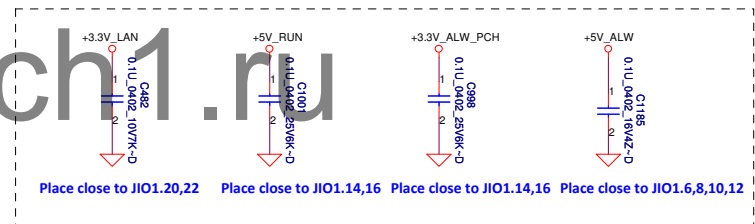
Default on,
WIRELESS_ON/OFF#:
LOW: ON
HIGH: OFF

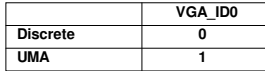


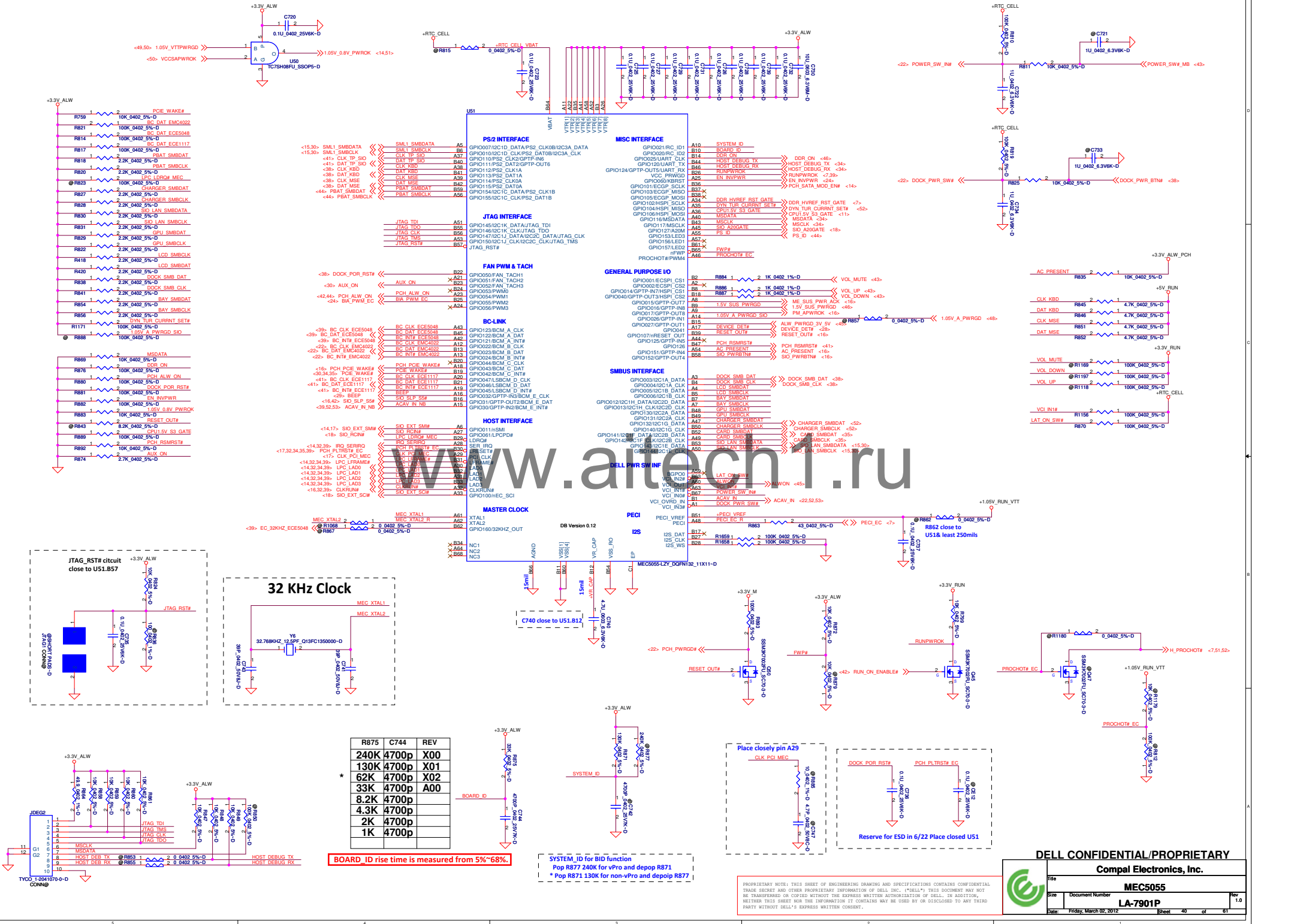
Pinout diagram for the E&T_1000K-F50E-04R connector. The diagram shows a 50-pin connector with pins numbered 1 to 50. The signals are as follows:

- Pin 1: +5V_ALW
- Pin 2: SIM_PWR
- Pin 3: UIM_CLK <34>
- Pin 4: UIM_RESET <34>
- Pin 5: UIM_VPP <34>
- Pin 6: UIM_DATA <34>
- Pin 7: (Unused)
- Pin 8: (Unused)
- Pin 9: (Unused)
- Pin 10: (Unused)
- Pin 11: (Unused)
- Pin 12: (Unused)
- Pin 13: (Unused)
- Pin 14: PCH_AZ_MDC_SDIN1 <14>
- Pin 15: PCH_AZ_MDC_SYNC <14>
- Pin 16: +3.3V_ALW_PCH
- Pin 17: (Unused)
- Pin 18: (Unused)
- Pin 19: (Unused)
- Pin 20: (Unused)
- Pin 21: (Unused)
- Pin 22: PCH_AZ_MDC_RST#
- Pin 23: PCH_AZ_MDC_BITCLK <14>
- Pin 24: (Unused)
- Pin 25: (Unused)
- Pin 26: (Unused)
- Pin 27: (Unused)
- Pin 28: RED_CRT <23>
- Pin 29: GREEN_CRT <23>
- Pin 30: BLUE_CRT <23>
- Pin 31: HSYNC_BUF <23>
- Pin 32: VSYNC_BUF <23>
- Pin 33: DAT_DDC2_CRT <23>
- Pin 34: CLK_DDC2_CRT <23>
- Pin 35: (Unused)
- Pin 36: (Unused)
- Pin 37: (Unused)
- Pin 38: (Unused)
- Pin 39: (Unused)
- Pin 40: (Unused)
- Pin 41: (Unused)
- Pin 42: (Unused)
- Pin 43: LAN_ACTLED_YEL#
- Pin 44: LED_100_ORG#
- Pin 45: LED_10_GRN#
- Pin 46: (Unused)
- Pin 47: (Unused)
- Pin 48: +5V_RUN
- Pin 49: (Unused)
- Pin 50: +3.3V_LAN

The diagram also shows the connector pin numbers 1-50 and the connector name E&T_1000K-F50E-04R.







R875	C744	REV
240K	4700p	X00
130K	4700p	X01
62K	4700p	X02
33K	4700p	A00
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

BOARD_ID rise time is measured from 5%-68%.

SYSTEM_ID for BID function
Pop R877 240K for vPro and depop R871
Pop R871 130K for non-vPro and depop R877

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MEC5055
LA-7901P

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The schematic diagram illustrates the electrical connections for the Touch Pad. It includes a +3.3V TP supply connected through resistors R902 and R903 to the DAT_TP_SIO and CLK_TP_SIO signals. These signals are also connected to the PS2 DAT TS and PS2 CLK TS inputs. The circuit features several capacitors (C751, C752, C753) and inductors (L54, L55) for signal conditioning. A diode bridge (D37) is used for power regulation, connected to +3.3V_ALW and +3.3V_RUN supplies. The output of the bridge is connected to the +3.3V_TP supply. The diagram also shows the connection of the Touch Pad module (JTP1) to the system, with labels for TP_CLK, TP_DATA, and TP_CLK signals.

BlueTooth

The diagram illustrates the electrical connection of a Bluetooth module. Key components and connections include:

- Power Supply:** A +3.3V_RUN supply is connected to the module.
- Resistors:**
 - R1133 and R1134 are pull-up resistors for the BT_COEX_STATUS2 and BT_PRI_STATUS signals, respectively.
 - R104, R105, R106, and R107 are pull-up resistors for the BT_COEX_STATUS2 and BT_PRI_STATUS signals, respectively.
- Connectors:**
 - JBT1 is a connector that interfaces the module's pins with the Link CTS module.
 - Link CTS is a module that provides a serial interface for the Bluetooth module.
- Signal Lines:**
 - BT_COEX_STATUS2 and BT_PRI_STATUS are status signals.
 - BT_DET# and BT_RADIO_DIS# are control signals.
 - COEX1_BT_ACTIVE and COEX2_WLAN_ACTIVE are active-low signals.
 - USBP11- and USBP11+ are USB differential signals.

Keyboard

Diagram illustrating the keyboard connection to the ACES_51524-0100N-001 connector (JKB1).

Pin connections:

- Pin 1: PS2 CLK TS
- Pin 2: PS2 DAT TS
- Pin 3: +3.3V_ALW
- Pin 4: +5V_RUN
- Pin 5: BC_INT#_ECE1117 <40>
- Pin 6: BC_DAT_ECE1117 <40>
- Pin 7: BC_CLK_ECE1117 <40>
- Pin 8: BC_CLK_ECE1117 <40>
- Pin 9: GND
- Pin 10: GND
- Pin 11: GND
- Pin 12: GND


Connector: ACES_51524-0100N-001 CONN@

Link CIS

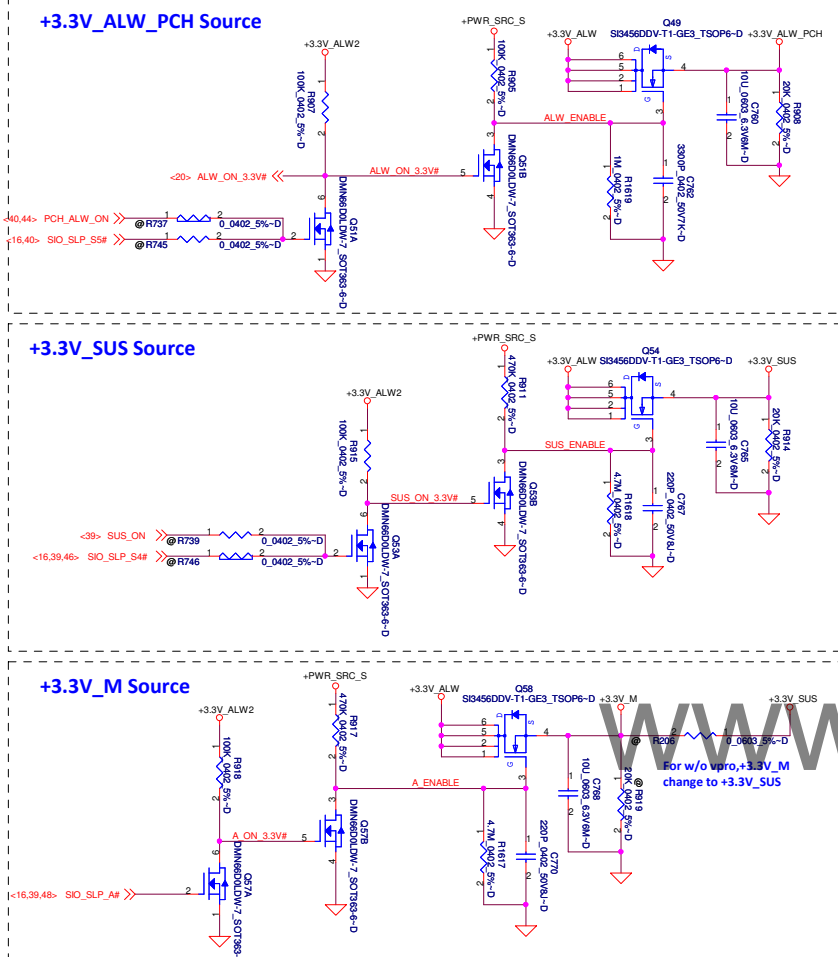
Decoupling capacitors:

- +3.3V_ALW: 0.1uF 0402 250VDC (C756)
- +5V_RUN: 0.1uF 0402 250VDC (C758)

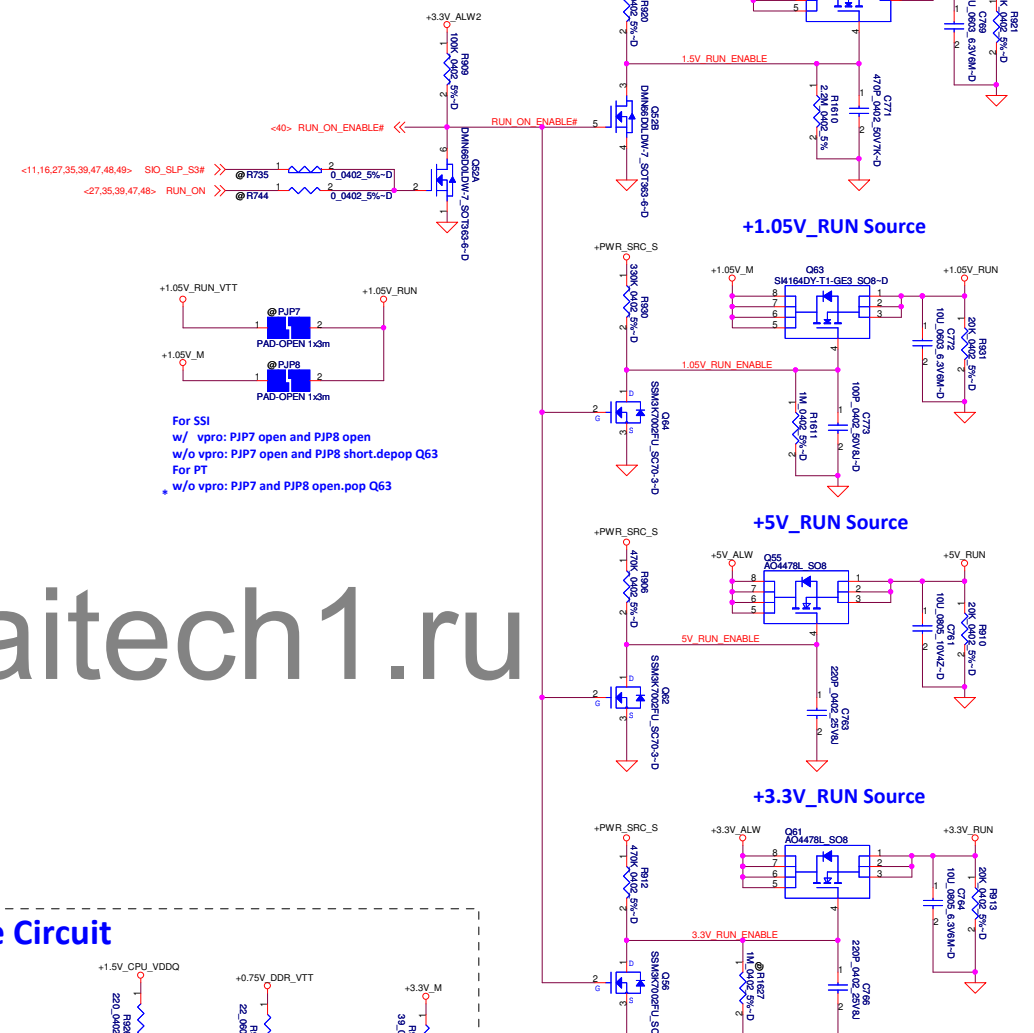
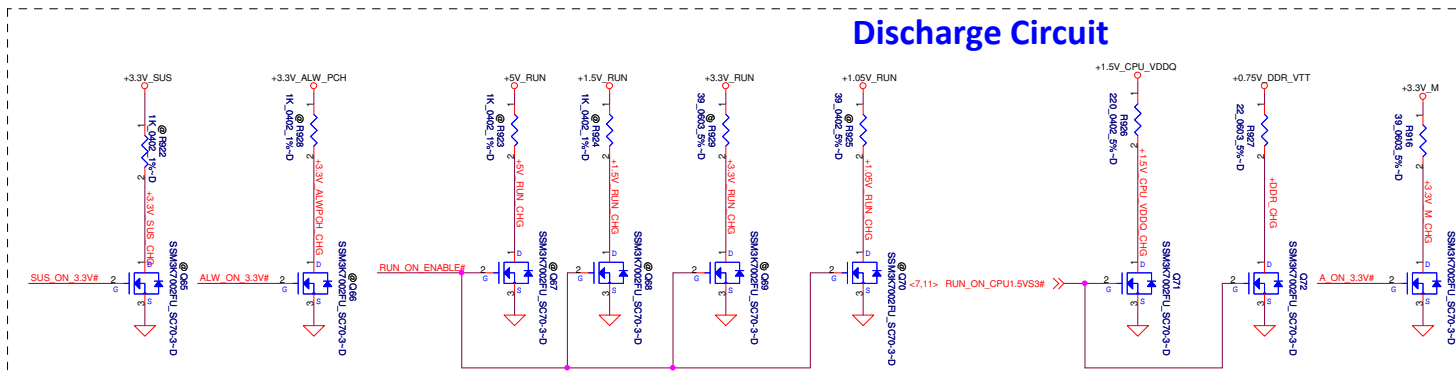
Place close to JKB1

	Compal Electronics, Inc.		
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	Int KB/TP/BT/RSMRST		
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DC/DC Interface



Discharge Circuit



For SSI
w/ vpro: PJP7 open and PJP8 open
w/o vpro: PJP7 open and PJP8 short, depop Q63
For PT
w/o vpro: PJP7 and PJP8 open, pop Q63

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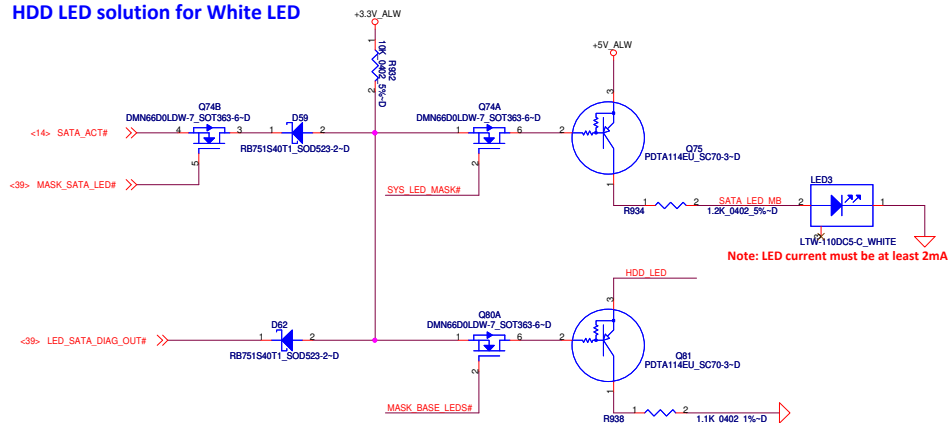
POWER CONTROL

LA-7901P

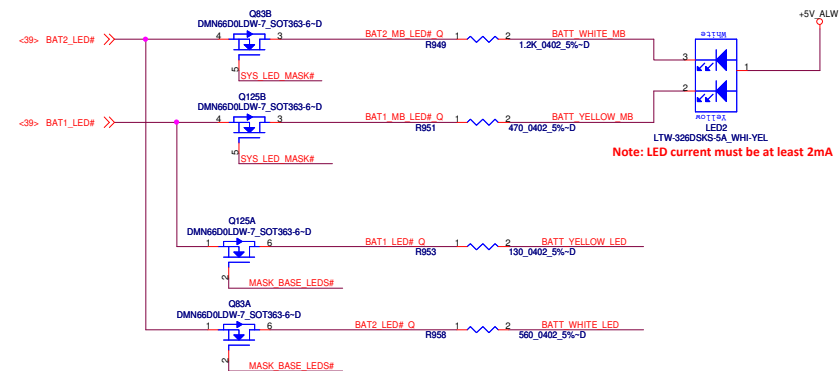
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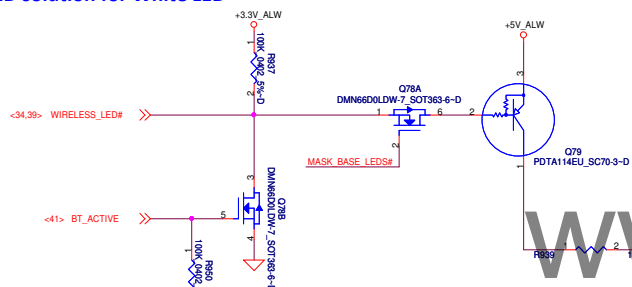
BDD LED solution for White LED



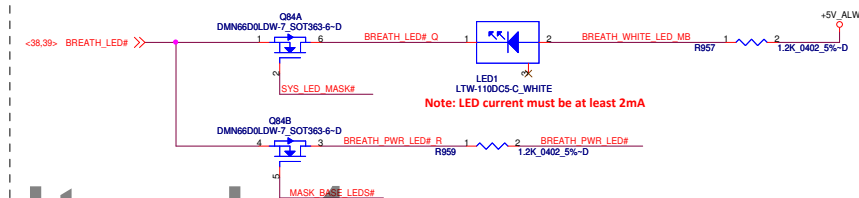
Battery LED



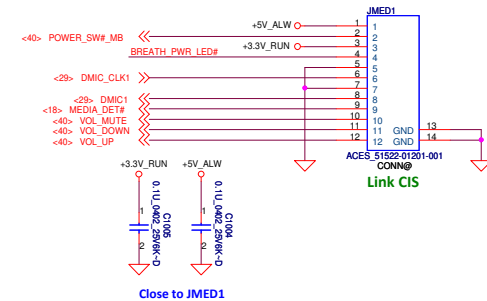
WLAN LED solution for White LED



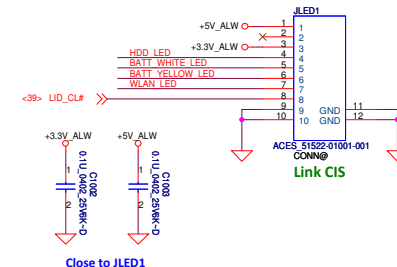
Breath LED



MEDIA BOARD



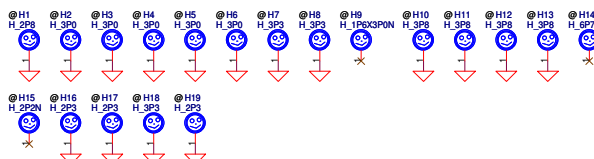
LED BOARD



LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

Fiducial Mark

- FD1
- FIDUCIAL MARK-D
- FD2
- FIDUCIAL MARK-D
- FD3
- FIDUCIAL MARK-D
- FD4
- FIDUCIAL MARK-D



EMI CLIP



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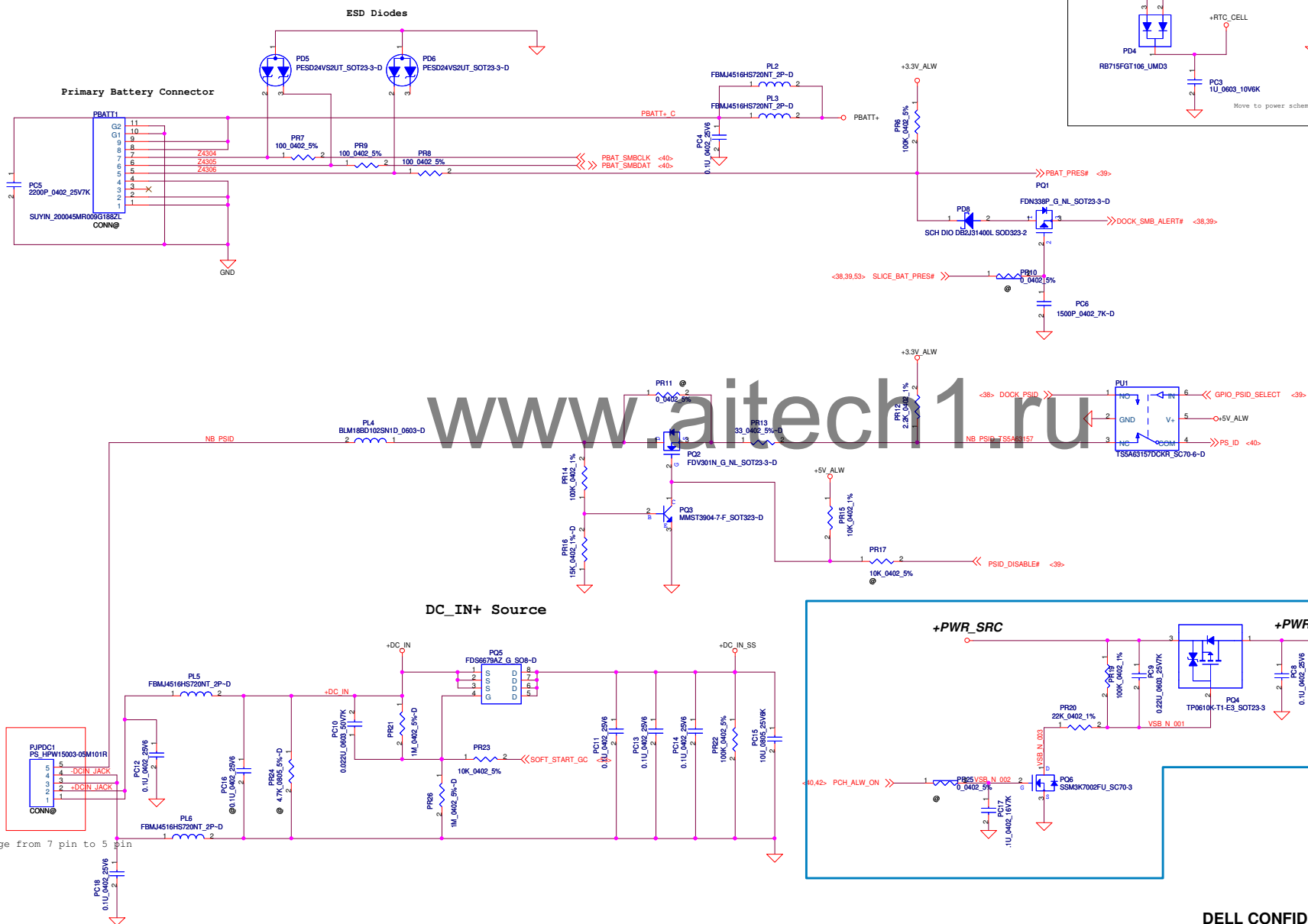
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Compal Electronics, Inc.

PWR/LED Conn/PAD/ME

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8/18 change from 7 pin to 5 pin

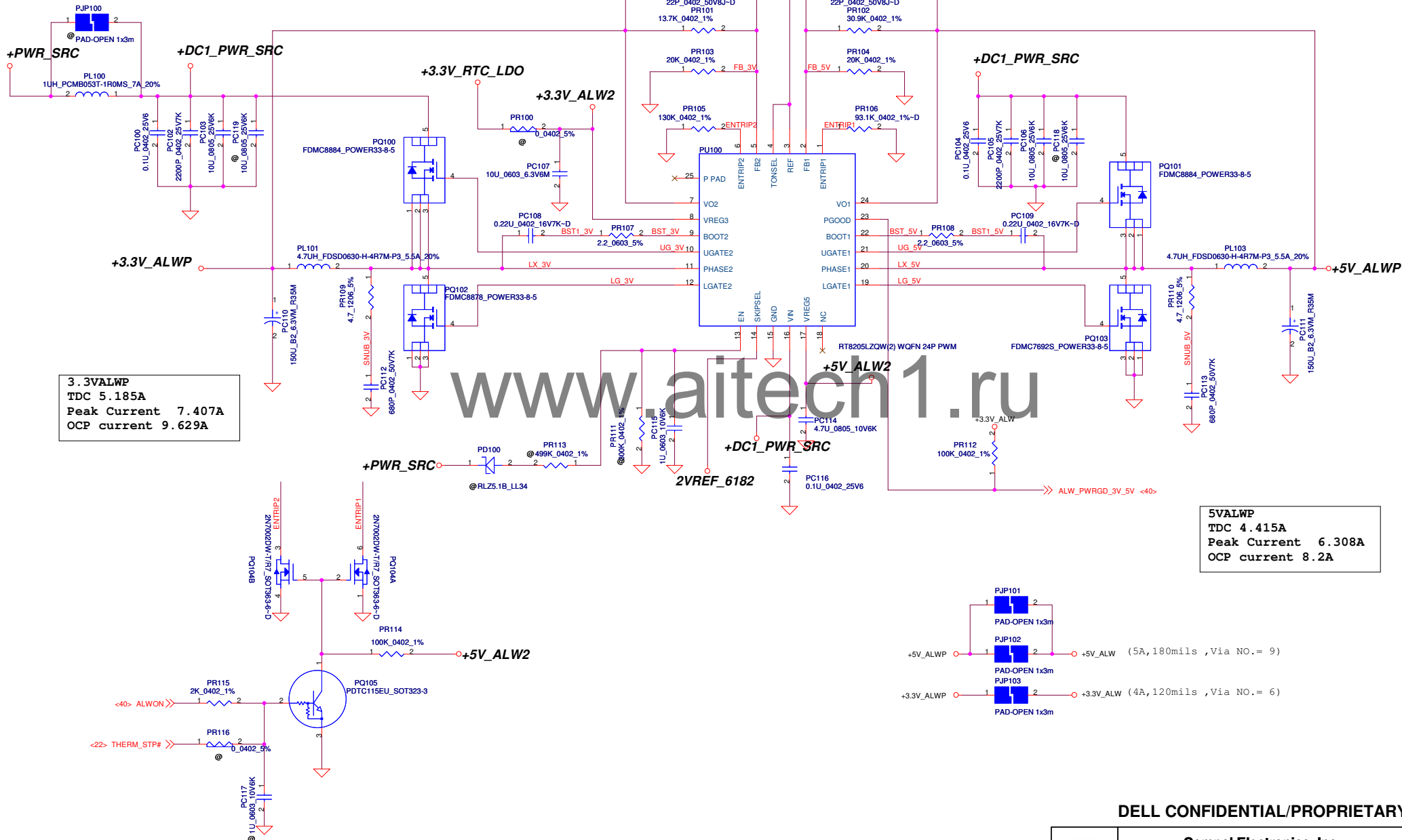
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+DCIN

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3.3VALWP
TDC 5.185A
Peak Current 7.407A
OCP current 9.629A

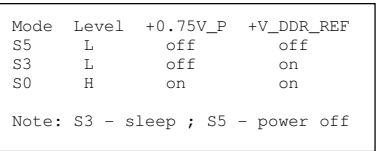
5VALWP
TDC 4.415A
Peak Current 6.308A
OCP current 8.2A

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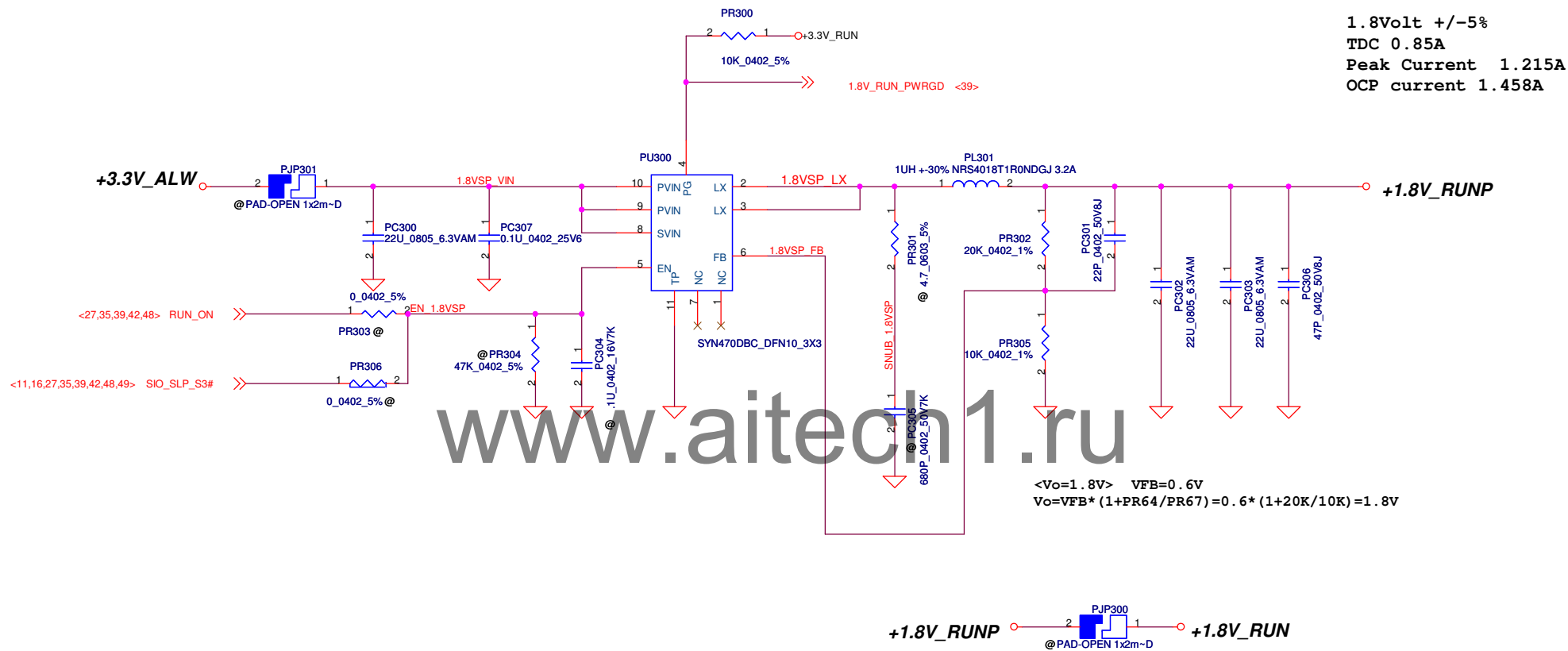
Compal Electronics, Inc.			
Title			
+5V_ALW/3.3V_ALW			
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```
0.75Volt +/- 5%
TDC 0.525A
Peak Current 0.75A
OCP Current 0.9A
```



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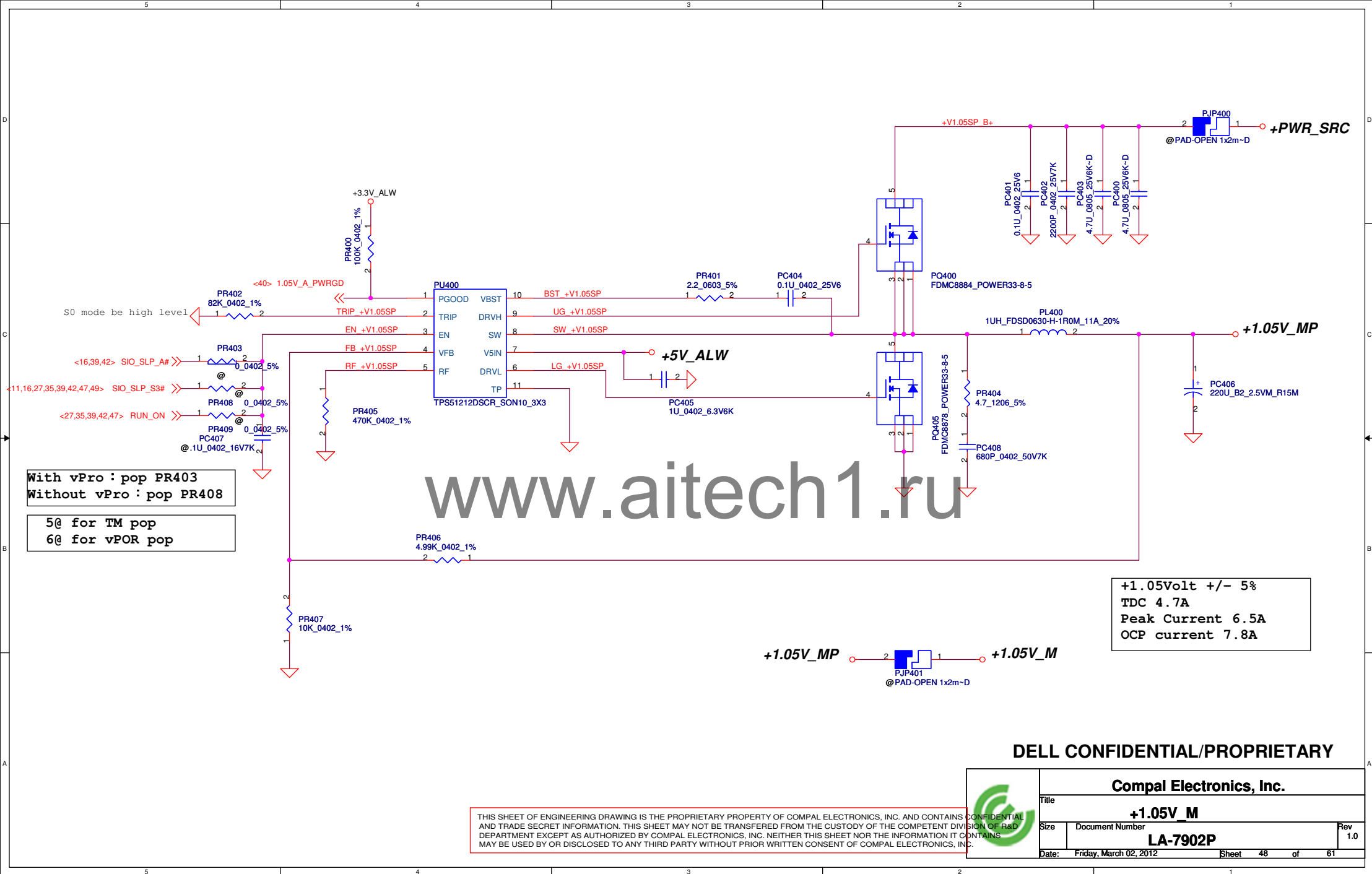
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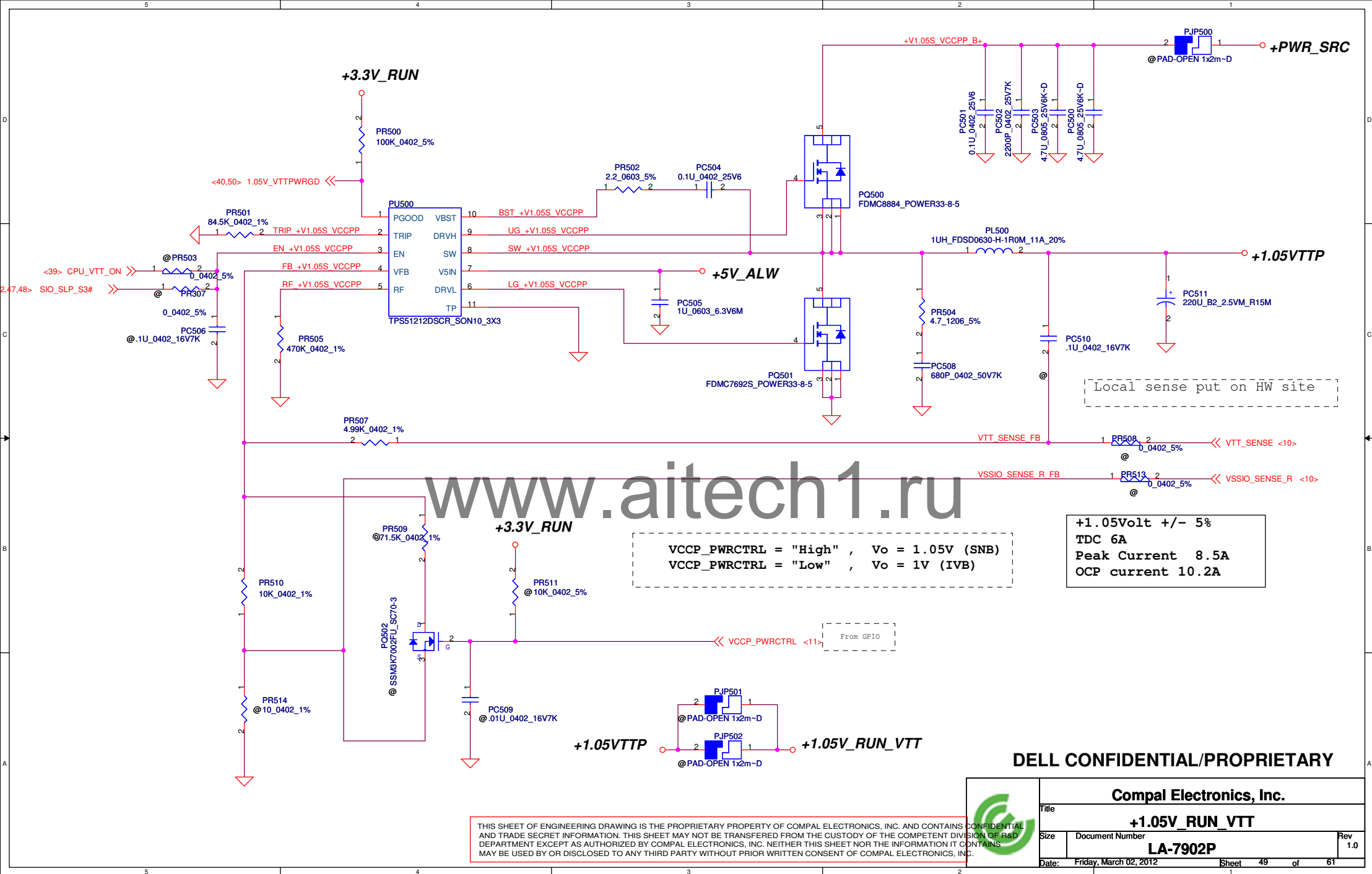


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Title			
+1.8V_RUN			
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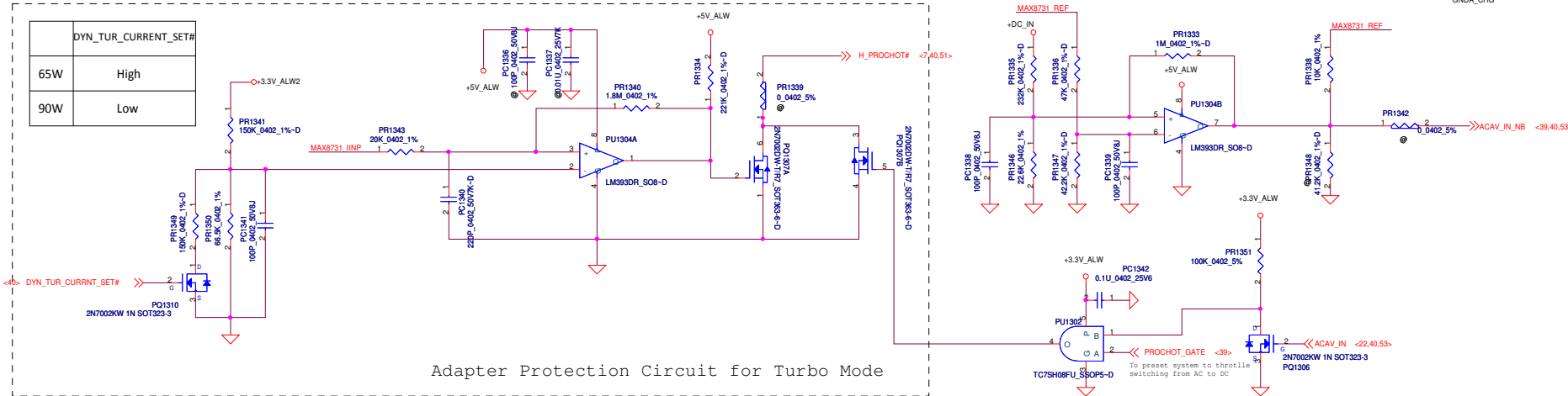
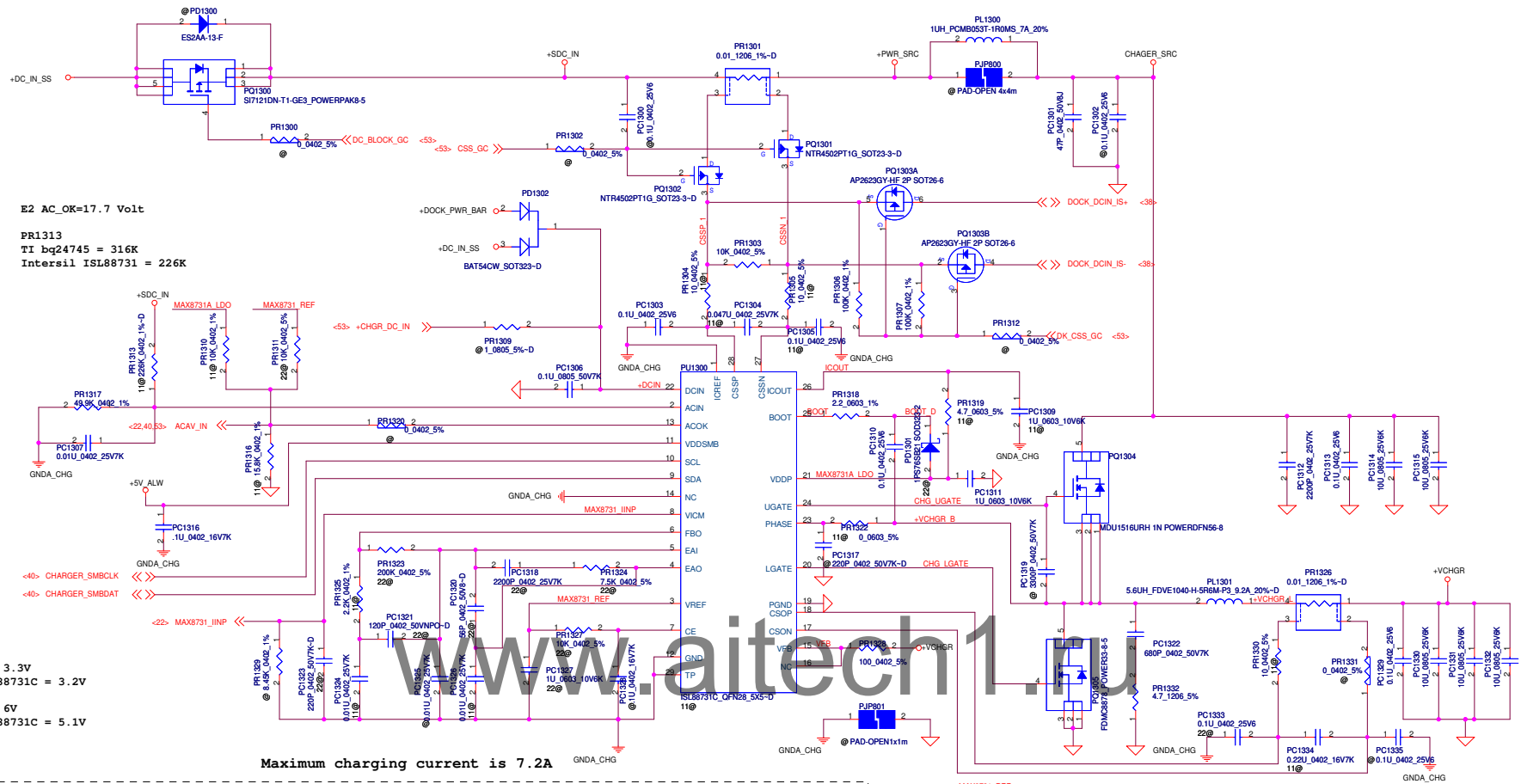




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Charger

LA-7902P

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	44	Power	8/18	Compal	ME design change.	PJPDC1 change from 7pin to 5pin	X01
2	45	Power	8/18	Compal	Main and 2nd IC common setting.	De-pop PD100,PR113,PR111	X01
3	45 46	Power	8/18	Compal	Prevent Jitter issue.	Add PC120,PC121,PC215 parallel with PR101,PR102,PR207	X01
4	51	Power	8/18	Compal	Prevent output voltage glitch when power up.	PU700 VCCP and VDD change form +5V_RUN to +5V_ALW	X01
5	53	Power	8/18	Dell	Change net name PBATT to SLICE_BAT_ON.	Change net name same as E4.	X01
6	50	Power	8/18	Compal	Reserve 0 ohm resistance for test.	Add PR90, PR91	X01
7	45 52	Power	8/30	Compal	For reduce EMI radiation.	Pop PL100, PL1300	X01
8	54	Power	8/30	Compal	Reserve cap for improve transient response.	Reserve PC1176	X01
9	53	Power	8/30	Compal	For reduce EMI radiation.	Add PC196, PC197, PC198, PC199, PC200	X01
10	54	Power	8/31	Compal	Change to green P/N.	Change PQ4, PC1153, PC1163, PC1164, PC1168, PC1169, PC1170, PC1171, PC1108, PC1109, PC1110, PC1187, PC1173, PC1174, PC1175, PC1157, PC1158, PC179, PQ1310, PQ1306 to green P/N	X01
11	48	Power	9/1	Dell	For support TL+TM	Change 6@ to pop for PC400~PC406, PC408, PL400, PQ400, PQ405, PR400~PR407, PU400. 5@ to @ for PR408.	X01
12	49	Power	9/1	Compal	For fix 1.05V_RUN_VTT on 1.05V	Depop PR509, PR511, PQ502. Change PR507 to 4.99k.	X01
13	51	Power	9/5	Compal	Follow EMI requirement.	Change PL700 to SM01000DJ00	X01
14	45 46	Power	9/6	Compal	Change to green P/N.	Change PC107, PC263, PC280, PC405, PC505 to HF P/N.	X01
15	52	Power	9/13	Compal	For reduce EMI radiation.	Pop PC1400~1404, PC1500~PC1504.	X01

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
16	51	Power	9/14	Compal	Adjust CPU transient , loadline and OCP	Add PC740 to 0.1uF Change PR750 to 365 ohm Change PR741 to 130K ohm Change PC744 to 3300pF, PR754 to 649ohm.	X01
17	51	Power	9/14	Compal	Adjust AXG transient , loadline and OCP	Change PR703 to 130K ohm Change PC709 to 82nF Change PR702 to 2.74K ohm Change PR711 to 383 ohm	X01
18	52	Power	11/17	Compal	Shortage issue	Change PQ1303 from NTGD416 to AP2623	X02
19	52	Power	11/17	Compal	Need ESD protected	Change PQ1306, PQ1310 from SB57002040L to SB000009Q80	X02
20	53	Power	11/17	Compal	IC version upgrade	Change PU11 from CD3301 to CD3301A	X02
21	45	Power	11/17	Compal	Shortage issue	Change PC110, PC111 from SGA00004E00 to SGA00002N80	X02
22	45	Power	11/17	Compal	EMI request	Pop PC1138, PC1139, PC1149, PC1150	X02
23	44	Power	11/21	Compal	Err 106 tier2 Fail issue	PWR_SRC_S control signal change from +3.3V_ALW to PCH_ALW_ON	X02
24	44	Power	12/05	Compal	Prevent COS.	Change PD8 from SCS0340L01L to SCS00005C00 Change PD1301 from SCS00003M0L to SCS0000400L	X02
25	54	Power	12/13	Compal	Prevent COS.	Change PC1176, PC1174, PC1173, PC1187, PC1157, PC1158, PC1165, PC1166 to SGA00002U1L	X02
26	50	Power	12/13	Compal	Improve efficiency	change PR86 to 22K_0402_5%	X02
27	47	Power	12/16	Compal	Prevent COS.	Change PL301 from SH00000MN00 to SH00000MW00	X02

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Title			
PWR_PIR 2			
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	11	HW	08/25/2011	COMPAL	INTEL review feedback	Add CC178,CC179,CC149,CC150	X01
2	14, 39	HW	08/25/2011	COMPAL	SMSC request to delete LPC_LDRQ0#	Leave LDRQ0# no connection on both of 5048 and PCH side Removed R743	X01
3	22	HW	08/25/2011	COMPAL	Removed reserve circuit for EMC4022	Removed R405,C280,R392,R394	X01
4	42	HW	08/25/2011	COMPAL	Load SW sources output rising time mismatch and COS. cost concern	Change back to E3 +3.3V/5V_RUN discrete solution Removed U78 and add Q55,Q61 circuit	X01
5	29	HW	08/25/2011	COMPAL	Codec is change to 92HD93	Pop R162~R166 and de-pop U73,R1540	X01
6	29	HW	08/25/2011	COMPAL	Reserve so lay with ALC290	Pop option for 92HD93/ALC290=>R1646/C1164; R1644/R1643; C965/R1642; Q107/R171 Reserve for ALC290 only: C1204, C1205, R1647, C1165, R1648 Reserve for 92HD93 only: R1645, C963 Add R174 depop and R175 pop	X01
7	20	HW	08/25/2011	COMPAL	Vgs less than cut-in voltage in battery mode	Add control circuit QH6,R279,CH107 for +5V_ALW_PCH	X01
8	27, 28	HW	08/25/2011	COMPAL	Vgs of 5V MOS maybe large than max rating	Add R517, R518	X01
9	11	HW	08/25/2011	COMPAL	Follow INTEL PDDG 0.8	De-pop RC140	X01
10	40	HW	08/25/2011	COMPAL	Change board ID to X01	Change R875 to 130Kohms	X01
11	34	HW	08/25/2011	COMPAL	PCH GPIO52 need 8.2~10K pull up +3.3VS	Change R695 from 100K to 10Kohms	X01
12	23	HW	08/25/2011	COMPAL	CRT SW 2nd source TI, TS3V713 pin29 is VDD	Connect U18 pin29 to +3.3V_RUN	X01
13	16	HW	08/25/2011	COMPAL	+1.05V_M turn off before APWROK de-assert	Add UH5,CH108 6@ circuit reserve for VPRO	X01
14	41	HW	08/25/2011	COMPAL	Reset IC threshold voltage issue	Change U4 to RT9801A (threshold adjustable) Add R1649~R1654;Reserve R1655 and pop R1623	X01
15	26	HW	08/25/2011	COMPAL	DPX_CA_DET voltage too low through dongle	Change U21 and U24 to SA000055G0L	X01
16	17, 18	HW	08/25/2011	COMPAL	Request from INTEL review feedback	Pop RH332 for PCH_GPIO3 and RH180 for GPIO27	X01
17	42	HW	08/25/2011	COMPAL	Material changed	Power team request Q59 change to SB00000L80L	X01
18	43	HW	08/25/2011	COMPAL	White light LED brightness is abnormal	Change R934, R938, R939, R949, R958, R957 and R959 to 1.2 Kohms	X01
19	40	HW	08/25/2011	COMPAL	Reserve C1208 for ESD backup plan	Reserve C1208 for ESD backup plan	X01
20	11	HW	08/25/2011	COMPAL	S3 can't resume issue	Control 1.5V_VDDQ by EC. Pop RC79 and de-pop RC82	X01
21	17	HW	08/25/2011	COMPAL	INTEL review feedback	Change RH331,RH272 to 10K ohm	X01

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
22	34	HW	08/25/2011	COMPAL	WWAN card request	JMINI1 pin 1 connect to PCIE_WAKE#	X01
23	14	HW	08/25/2011	COMPAL	ROM size changed	Change U52 to 8M and R936,R895,R897,R900 to 6@	X01
24	11	HW	08/25/2011	COMPAL	Material package changed	Change CC161~CC166 from 0402 to 0603	X01
25	42	HW	08/25/2011	COMPAL	BOM changed	Change Q60 to 6@	X01
26	39	HW	08/25/2011	COMPAL	GPIO signal name changed same as E/P	Change PBATT_OFF to SLICE_BAT_ON	X01
27	34	HW	08/25/2011	COMPAL	Material package changed	Changed C615 to SF000002000	X01
28	30	HW	08/26/2011	COMPAL	LAN EA result	Changed RL23 to 1.2K Ohm.	X01
29	40	HW	08/26/2011	COMPAL	Backdrive issue	Depop R1169,R1197,R118 due to it has internal pull high.	X01
30	37	HW	08/29/2011	COMPAL	To avoid power short to GND	NC Pin 15 for JAUD1	X01
31	37	HW	08/30/2011	COMPAL	Follow connector list	Swap JAUD1 pin.	X01
32	12	HW	08/30/2011	COMPAL	Change part to HF part	Change QD1, QD2 part number to SB501380050 (for HF)	X01
33	15	HW	09/01/2011	COMPAL	For clock EA	Change RH311 and RH314 to 10 ohm	X01
34	43	HW	09/01/2011	COMPAL	ME drawing update	Add H19	X01
35	14, 16 19, 22 30, 40 42	HW	09/01/2011	COMPAL	BOM option change for TL	Change U53,R936,R895,R897,R900,RH350,UH5,CH108,RH116 RH202,R385,R426,R402,Q63,R931,Q58,Q60 R916,RL46,R871 to pop Change RH359,RH321,RH119,RH204,R430,R386,R408 ,R206,RL47,R877,to depop	X01
36	25	HW	09/02/2011	COMPAL	Due to EMI HDMI test Fail, add EMI solution	Change resistor to Inductor Change R451, R459, R462, R466, R468, R469, R470, R471 to 9nH L99, L100, L101, L102, L103, L104, L105, L106. Add C1209, C1210, C1211, C1212, C1213, C1214, C1215 and C1216 between Inductor and HDMI connector	X01
37	37	HW	09/05/2011	COMPAL	ME connector list change	Change JAU1 to 50271-0020N-001	X01
38	37	HW	09/06/2011	COMPAL	EMI issue	Add L107 & R1656,R1657	X01
39	15,30	HW	09/06/2011	COMPAL	Follow LL to reserve SM bus for BRCM LAN	Add QH8,RL50,RL51	X01
40	36	HW	09/08/2011	COMPAL	Follow Intel design guide	Change C412~C415 to 0.1uF for USB3.0 signal	X01
41	7	HW	09/08/2011	COMPAL	Follow ESD recommand.	Reserve CC1141~CC144 for ESD	X01
42	14,15,40	HW	09/08/2011	COMPAL	Crystal EA result	Change CH2,CH3 to 18pF Change C741,C743 to 39pF Change CH18,CH19 to 10pF Change CL5,CL6=33pF,RL22=510 ohm	X01

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43	29	HW	09/13/2011	COMPAL	Follow IDT recomment	Swap R169~R172,C973~C976 connection	X01
44	42	HW	09/13/2011	COMPAL	Change Q55,Q61 part for open soldering issue.	Change Q55,Q61 from DMN3030LSS-13 to AO4478L	X01
45	40	HW	10/13/2011	COMPAL	Change board ID to X02	Change R875 to 62Kohm	X02
46	42	HW	10/13/2011	COMPAL	Rated Vgs of Q61 is 25V	De-pop R1627	X02
47	39	HW	10/13/2011	COMPAL	SMSC change 5048 pin A23 to GPIOI0	Re-link ECE 5048 symbol	X02
48	40	HW	10/13/2011	COMPAL	SMSC review feedback	Reserve R1658 and R1659 100Kohms to GND for I2S disabled	X02
49	41	HW	10/13/2011	COMPAL	Change reset IC to RT9818A-44GU3	Update U4 symbol and add R1629 for backup of inrush prevention. Change RSMRST# pull up with 100Koms. Pop R1655 and de-pop R1623.Delete R1649~R1654	X02
50	39	HW	10/13/2011	COMPAL	When suspend/resume cycles, wireless SW GPIO IRQs keeps giving	Change pull up rail to +3.3V_ALW for WIRELESS_ON#/OFF	X02
51	29	HW	10/13/2011	COMPAL	15" UMA speaker no sound issue	Pop snubber on speaker trace with C: 2200pF and R: 3.3ohms. Change bead rated current from 200mA to 2A.	X02
52	29	HW	10/13/2011	COMPAL	EMI request	Pop C981,C982,C983,C985,C986,C987	X02
53	27	HW	10/13/2011	COMPAL	Depop HDD control power circuit for cost down.	Depop R1624,Q28,R500,R499,R617,C393	X02
54	30	HW	10/18/2011	COMPAL	Crystal EA result	Change YL1 to 3G025000FA1H, CL5,CL6 to 12pF.RL22 to 200 ohm.	X02
55	All	HW	10/18/2011	COMPAL	For cost saving.	Change 0 ohm to R-short.	X02
56	42	HW	10/26/2011	COMPAL	1V leakage on 3.3V_RUN during system boot	Pop Q69 and R929	X02
57	42	HW	10/26/2011	COMPAL	Inrush current with Smart Card detect fail issue	change C763 and C766 to 2200p	X02
58	43	HW	10/27/2011	COMPAL	LED Conn PIN definition change	JLED1 PIN define change	X02
59	37	HW	10/27/2011	COMPAL	Remove 2pin connector for Audio performance	Remove JAG1 2 pin connector.	X02
60	42	HW	11/01/2011	COMPAL	Change MOSFET to wihtout Schottky Diode for +1.5V_RUN leakage issue	change QC3, Q59 as AO4304L from AO4728L	X02
61	14	HW	11/15/2011	COMPAL	RTC issue	change CH2, CH3 to 15pF	X02
62	14	HW	11/15/2011	COMPAL	S5 power consumption over spec.	depop RH288	X02

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63	34	HW	11/29/2011	COMPAL	S3 had leakage in +3/5V_RUN	De-pop R725, remove R695 and add +3.3V_RUN pull high at PCH side(RH361)	X02
64	32	HW	11/29/2011	COMPAL	TPM is changed to AT97SC3204-X2A18-AB	U39(TPM) is changed to SA00004WQ10 (AT97SC3204-X2A18-AB) for WIN8 support	X02
65	32	HW	11/29/2011	COMPAL	+3.3V_RUN Giltch when AC plugin	Add D87, R1662 and R1663 (pull high to +3.3V_RUN_TPM) for HW solution backup	X02
66	14~21	HW	11/29/2011	COMPAL	Change PCH to C1 version	Change UH4 to SA00005AG1L(HM77 for non vpro)	X02
67		HW	11/29/2011	COMPAL	Change RC value at Gate of MOS Load SW to modify power rail soft start timing	RC72 from 100K to 330K; RC143 form 330K to 1M; CC136 form 0.1u to 0.022u R412 from 100K to 470K; R1632 form 1M to 4.7M; C293 form 0.1u to 0.022u R507 from 100K to 470K; R517 form 1M to 4.7M; C400 form 0.1u to 0.022u R722 from 100K to 470K; R1625 form 1M to 4.7M; C644 form 4700p to 220p R729 from 100K to 470K; R1628 form 1M to 4.7M; C650 form 4700p to 220p R917 from 100K to 470K; R1617 form 1M to 4.7M; C770 form 4700p to 220p R920 from 100K to 470K; R1610 form 470K to 2.2M; C771 form 4700p to 470p R930 from 100K to 330K; R1611 form 470K to 1M; C773 form 2200p to 100p R906 from 100K to 470K; C763 form 2200p to 220p R912 from 100K to 470K; C766 form 470p to 220p	X02
68	36	HW	12/01/2011	COMPAL	Change P/N for HF	Change C412~C415 P/N to SE076104K8L	X02
69	35	HW	12/01/2011	COMPAL	Reserve 0.1uF CAP to GND for ESD request	reserve CE14, CE20, CE22, CC151, CC152, CC153 to GND	X02
70	19	HW	12/05/2011	COMPAL	Change LH1 from bead to Inductor for CRT	Change LH1 to 1uH Inductor(SHI00007W0L)	X02
71	17, 38	HW	12/07/2011	COMPAL	EMI solution for E-Docking USB port	Swap USB Port7 and Port8 and reserve a choke(L108) at E-Docking side; Port7 from NA to E-docking Port8 from E-Docking to NA	X02
72	24, 32, 37	HW	12/07/2011	COMPAL	Change USB9,12,13 CMC to 180ohm for EMI request	Change L10,L52,L107 to SM070002X00(OCF2012181YZF)	X02
73	37	HW	12/08/2011	COMPAL	Follow CONN List_1130A Change JAUD1 to ACES_51522-0200N-P01	Change JAUD1 to ACES_51522-0200N-P01	X02
74	22	HW	12/09/2011	COMPAL	Thermal requests to change OTP from 88 to 92	Change R406 from 953ohm to 1.24Kohm	X02
75	41	HW	12/09/2011	COMPAL	To prevent inrush current at reset IC input	Change R1629 from 0ohms to 33ohms resistor	X02
76	19	HW	12/09/2011	COMPAL	For CRT issue	Change CH36 from 10uF to 22uF	X02
77	25	HW	12/13/2011	COMPAL	Change HDMI R,C value for EMI request	Change R448,R449,R450,R452,R453,R454,R455,R456 from 680ohm to 604ohm; C1209~C1216 from 4.7pF to 3.9pF	X02
78	42	HW	12/15/2011	COMPAL	+3.3V_SUS sequence timing	R911 from 100K to 470K; R1618 from 1M to 4.7M; C767 from 4700p to 220p	X02
79	43	HW	12/15/2011	COMPAL	Change current limit resistors of LED	R934 from 1.2K to 820, R957 from 1.2K to 1K, R951 from 330 to 270, R949 from 1.2K to 910,	X02

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80	34	HW	01/04/2012	COMPAL	Change RC25 value for ESD	Change RC25 from 0ohm to 1kohm(ST MEMO)	A00
81	40	HW	01/17/2012	COMPAL	SMSC creates a new catalog part number and IC marking for the MEC5055	Change U51 P/N to SA00003TZ2L	A00
82	43	HW	02/20/2012	COMPAL	Change current limit resistors of LED	Change R938 to 1.1k ohm, R958 to 560 ohm, R953 to 130 ohm, R951 to 470 ohm, change R939, R959, R957, R934, R949 to 1.2k ohm	A00
83	38	HW	02/24/2012	COMPAL	Dalmore14 UMA hang on white screen issue when attached AC+media battery after hot dock.	Change R755 from 100k ohm to 10k ohm	A00
84	40	HW	02/24/2012	COMPAL	Change board ID to A00	Change R875 to 33K ohm	A00
85	33	HW	02/24/2012	COMPAL	Change SD CLK damping resistor for EMI request	Change R676 from 33 ohm to 10 ohm	A00
86	32	HW	02/24/2012	COMPAL	Change BOM option for TPM/TCM funtion	Change C550,C551,C552,C553,R659,R660,R1662,RH311 BOM option to 5@	A00
87	25	HW	03/03/2012	COMPAL	SMT request to change F2 footprint	For DFX concern of F2 2nd source, SP040003H0L, change F2 footprint to F_MF-MSMF050-2	A00
88	14~21, 30	HW	03/03/2012	COMPAL	Change PCH P/N for X-build	UH4 is changed to SA00005AG3L	A00
89	14	HW	03/03/2012	COMPAL	De-pop resistor on PCH JTAG for power saving	De-pop RH288, RH47, RH48 and RH49	A00

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